ELEC 599 REPORT

MODELING OF WELKIN RF IN A DSSS SYSTEM FOR WCDMA APPLICATIONS

By

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ABSTRACT

In this report, the author studied the methodology of distortion-true software modeling for RF (radio frequency) in a DSSS W-CDMA system. A complete end-to-end testbed based on the Welkin RF system is built by SystemView with specifications from real world RF components. This testbed includes digital baseband transmitter, RF transmitter, wireless channel, RF receiver, and baseband receiver for WLAN applications. Several implementation issues will be discussed. Various time/frequency domain analysis methods help to understand the non-linearity of real RF components in each stage and provide a reference to the hardware design. To support the capability of multi-domain simulation, Matlab custom tokens were integrated. The simulation results show the effects of noise figure introduced by RF on the receiver's sensitivity.

1. INTRODUCTION

Wireless networking is growing fast now. The change from mainly professional wireless applications(military, private mobile radio, etc.) to a consumer market has severe implications for the total design process. There are a lot of tradeoffs among the channel coding, modulation schemes and the design of RF transceiver. These factors relate closely to the cost and complexity of the transceiver. Unfortunately, it is difficult to generate a close mathematical form for all these tradeoffs because of the complexity. In general, the modulation, interference, and implementation of time-varying effects of channels as well as performance of specific demodulator are analyzed as a complete system using simulation to determine relative performance and ultimate selection.

Currently, people at **CMC (Center for Multimedia Communications)** of Rice University are investigating advanced coding, modulation and equalization techniques especially for the indoor wireless channel using sophisticated diversity techniques, such as multiple transmit and receive antennas. Implementation issues of orthogonal frequency division multiplexing **(OFDM)** are also studied. A **RENE** project (Rice Everywhere Network) which aims to provide multi-tier wireless networking service is ongoing now [19].

In order to advance the development of an advanced multitier wireless physical layer prototype, simulation and algorithm mapping must proceed through several design stages. Initial algorithm design and simulation will occur with high level environments such as **Simulink/Real Time Workshop** from the **Mathworks** and Signal Processing Workstation(**SPW**) from **Cadence**. From the high level simulation, insights will be gained on appropriate approximations and algorithm mappings suitable for DSP processors. A general W-CDMA testbed based on Simulink and TI's DSP has been developed [45].

Fig. 1.1. RF Interface in the RENE Project

Fig. 2.1 Multi-disciplinary Requirement of RF Design/ Modeling

However, virtually all these work were done only on baseband. It is clear that a complete system is more than DSP. To verify the schemes accurately, a complete system with RF section is in critical demand. With this knowledge, the RENE targets to develop a universal RF interface(Fig.1.1.) for a wireless network interface card(WNIC) to support multi-tier service. In the first stage the Welkin RF prototype will be used.

Although the RF part of these systems constitutes only a minor part of the total design area, it presents a major challenge in the total design cycle. This challenge is caused not only by the analog/RF nature of the design but also by the lack of the appropriate tools, models and design flows.

Since the hardware is still not available, there is a good demand to evaluate the design and build some software simulation on RF, if possible. The main purpose of this summer 599 project is to understand the design of Welkin RF section and build our expertise on RF, while providing design considerations to the baseband schemes. This technical report is a summary of the current work and a prospective of the future direction.

In section two, the author first introduces some basic but essential concepts in RF design and modeling. Nonlinearity effects of the RF circuits are emphasized here. The diagram of the welkin design is reviewed briefly in section 3. In section 4, several simulators supporting RF simulation are reviewed and commented. Using the PC-based system level simulator **"SystemView"** from elanix(www.elanix.com), a complete W-CDMA testbed including the RF section based on the **Intersil Prism II**(www.intersil.com) chip set **HFA3683A** was built based on the two-page diagrams from welkin system. Baseband schemes will be added for completion of the system based on W-CDMA specification. Several design details will be discussed here. Although the most direct merit of a communication system is the BER (bit error rate) curve, it will be a great help to view the features of signals in each stage of the system. So a cascaded analysis of the system will be carried both in time and frequency domain. Some other special analysis tools such as eye-diagram and I-Q scattering plot will also be used to evaluate the performance.In the next section, the author will discuss some design considerations for a practical RF system. Requirements components will be described and the advantages of the current design will be commented. At last, the author will derive a new methodology which provides a multi-platform testbed for a complete end-to-end system with distortion true simulation of RF circuit.

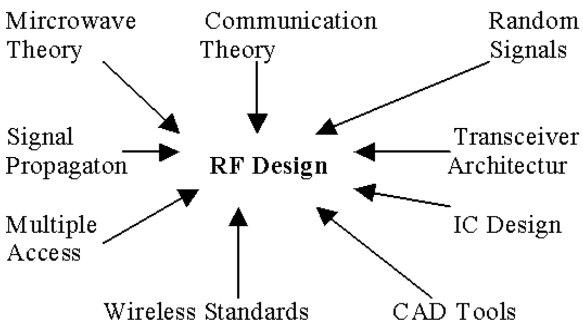


Fig. 1.1. RF Interface in the RENE Project

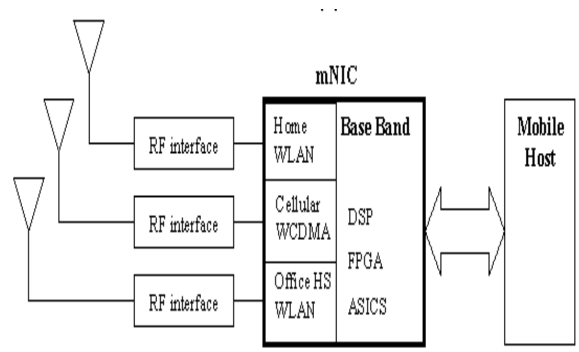


Fig. 2.1 Multi-disciplinary Requirement of RF Design/ Modeling

2. BASIC CONCEPT FOR RF MODELING

2.1 Challenge of RF Modeling

The accuracy of a simulation depends on three factors: the accuracy of the models, the error injected by the simulator algorithms and the circuit itself. If the models do not accurately reflect the physical effects that are important to the circuit behavior, then the answer will be wrong. Similarly, if the model does not match the physical device because the model parameters are poorly chosen, again the answer will be in error. However, even if the model does a good job of the reproducing the important characteristics of the device, the simulator itself can inject error into this solution.

In contrast to other types of analog and mixed signal circuits, RF systems demand a good understanding of many areas that are not directly related to integrated circuits (ICs). Figure 2.1 from [16] explains this situation clearly. Most of these areas have been studied extensively for more than half a century, making it difficult for an engineer to acquire the necessary knowledge in a reasonable amount of time. Even at present, the literature pertaining to RF design appears in more than 30 journals and conferences. Traditional wireless system design has been carried out at somewhat disjointed levels of abstraction: RF system experts plan the transceiver architecture; IC designers develop each of the building blocks; communication theory people derive their baseband coding/modulation schemes with a simple channel model. As the industry moves toward higher integration and lower cost, RF and wireless design demands increasingly more "concurrent engineering".

There are a lot of tradeoffs involved in the design of RF circuits, which must process signals with a wide dynamic range at high frequencies. These tradeoffs can be shown in the RF design hexagon (Fig.2.2.), proposed by Behzad Razavi in[16].

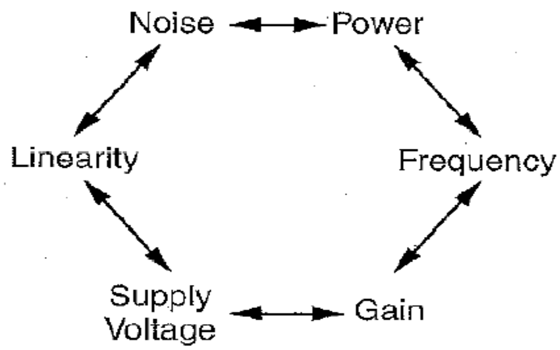


Fig. 2.2 Tradeoff Hexagon in RF Design/Modeling

An RF circuit forms the link between some baseband information signal and an antenna. A trasmitter modulates the baseband signal on a high frequency carrier(sinusiod) and the task of the receiver is to retrieve the baseband signal from the modulated carrier Thus as compared to baseband circuits, RF circuits are special in the sense that signal that they process modulated carriers. In the frequency domain a modulated carrier is a narrow band signal where the absolute bandwidth is related to the frequency of the carrier signal and the relative bandwidth is related to the modluating baseband signal. Practically, the ratios of the two frequencies is in the order of 100 or 1000.

Another major difference is that in RF systems, noise is a mojor issue. Noise consists of the small unwanted signals in a system. One can think of several forms of device noise(thermal noise, shot noise, flicker noise) but also of interferers like neighbouring channels, mirror frequencies, etc. All noise sources are of major imporantce because they directly translate to bit-error-rates of the transmitted data. Therefore it is imperative that RF designers can predict the overall noise quickly and accurately.

When dealing with narrow band signals in a noisy environment two mechanisms are of major importance. Firstly, if a narrow band signal is passed through a non-linear component, the spectrum will be repeated about integer multiples of the carrier frequency resulting in a very wide but ‘sparse’ spectrum. Secondly, the signal will interact with other signals in the circuit leading to wanted and unwanted frequency shifts.

Although the non-linearity of RF circuits has been explained comprehensively in [16], they are so essential that we put it here for emphasis and completion.

2.2 Non-linearity

The non-linearity effect is shared by virtually all RF circuits. For simplicity, we only discuss three-order non-linearity here. Assuming a sinusoidal input applied to a nonlinear system, the non-linear effect can be formulated by a polynomial. This causes the following effects.

Harmonics

$$\begin{aligned} y(t) &= \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \\ &= \alpha_1 \cos \omega t + \alpha_2 \cos^2 \omega t + \alpha_3 \cos^3 \omega t \\ &= \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{3\alpha_3 A^3}{4}) \cos \omega t + \frac{\alpha_2 A^2}{2} \cos 2\omega t + \frac{\alpha_3 A^3}{4} \cos 3\omega t \end{aligned} \tag{1}$$

Clearly now this introduces the harmonics components. We make two observations here, 1st, the even order harmonics results from α_j with even j and vanishes with odd symmetry; 2nd, by assuming the signal with small amplitude, the nth order harmonics can be approximated to be proportional to A^n .

Gain Compression

A lot of RF components share the effect of gain compression. When a component is saturated, it suffers from compression in the high gain. A measure people always use in the literature is the 1-dB compression point. This means the maximum input point when the output is dropped by 1-dB from the linear gain. This is indicated by Fig. 2.2. In the specification of RF components, this measure can be either input P1dB or output P1dB, according to different type of interests. The relation can be derived directly from the physical concept as: *Output P1dB = Input P1dB +Gain-1dB.*

Desensitization and Blocking

The desensitization and blocking effect occurs when a small desired signal is processed along with a strong interference. Assuming the input as $A_1 \cos \omega_1 t + A_2 \cos \omega_2 t$ contains two frequencies, and A1<< A2, where A2 is interference and A1 is desired signal. Then the output *y(t)* is

$$y(t) = (\alpha_1 + \frac{3}{2}\alpha_3 A_2^2) A_1 \cos \omega_1 t + \ldots \tag{2}$$

Then for α_3<0, the gain may drop to zero, which means blocking the weak desired signal. Conceptually, it means the strong interferer makes the circuit less sensitive to weak signals.

Cross Modulation

Also consider the input as two signals. If the interferer is modulated by a sinusoid, like $A_2(1+m\cos\omega_m t)\cos\omega_2 t$, the modulation can be transferred to the amplitude of weak signal, as Equ.3. expresses. Thus the desired signal at the output contains amplitude modulation as a function of ω_m. This is called cross modulation and may occur in the case of simultaneous independent channels.

$$y(t) = \alpha_1 A_1 + \frac{3}{2}\alpha_3 A_1 A_1^2 f(m, \omega_m) \cos \omega_1 t + \ldots \tag{3}$$

Intermodulation

This phenomenon arises from mixing of the two signals when their sum is raised to a power greater than unity. Assume the input as $x(t) = A_1 \cos\omega_1 t + A_2 \cos\omega_2 t$, then the output can contain a lot of intermodulation products at $\omega_1 \pm \omega_{2,} 2\omega_1 \pm \omega_2, and\ 2\omega_2 \pm \omega_1$. This is called intermodulation. Since the third-order IM at $2\omega_1 - \omega_2, and\ 2\omega_2 - \omega_1$ are close to the fundamental frequency, they can become strong interferences and are of particular interest. A calculation of these components shows that the third-order IM products increase in proportion to *3logA* in the sense of *dB*. Ploted on a logrithmic scale, the magnitude of the IM products grows at three times the rate of the fundamental frequency (Fig.2.3).

Noise Figure

In RF design, even though the ultimate goal is to maximize the SNR for the received and detected signal, most of the front-end receiver blocks are characterized in terms of their “noise figure”. There is a pair of definitions. F is defined in linear scale as “noise factor”, while in dB scale it is called “ noise figure”.

$$NF = 10 \log(SNR_{in} / SNR_{out})$$

$$F = SNR_{in} / SNR_{out} \tag{4}$$

For cascaded components, there is a derived equation to compute the overall noise figure,

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \ldots + \frac{NF_n - 1}{G_1 G_2 \ldots G_{n-1}} \tag{5}$$

In this equation, *Gi* is the gain of each stage. Actually the transceiver is always too complicated to calculate the NF with this equation. But this equation is always used to analyze and estimate the possible NF in the process of design, thus providing criterion to select components. In the later sections, we will discuss this issue in more details.

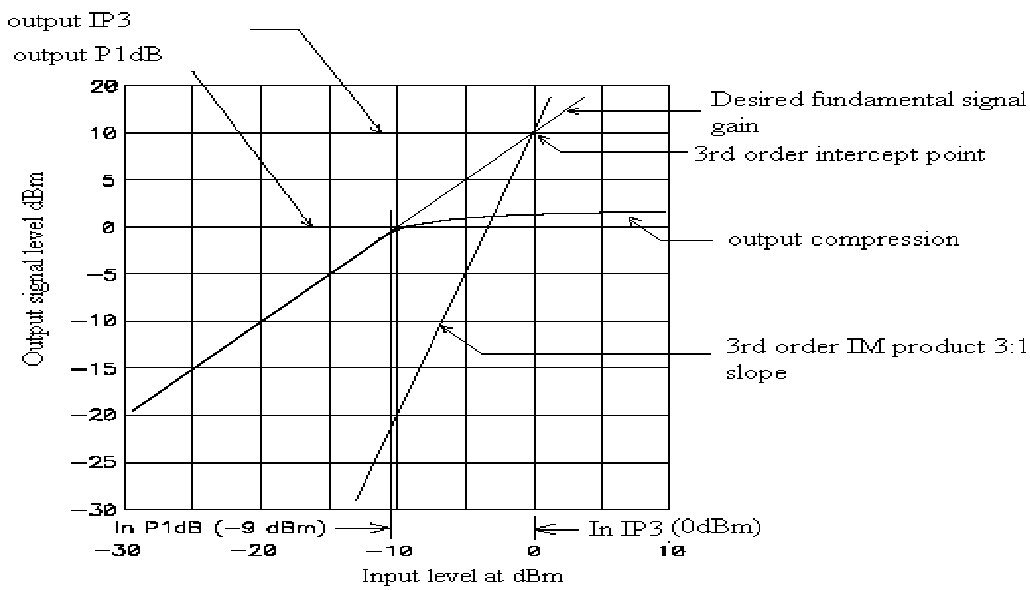


Fig.2.3 Nonlinearity Effects of RF Circuits: P1dB Compression and IP3

3. WELKIN RF SYSTEM

This section describes briefly the Welkin RF system shown in Fig.3.1 and Fig.3.2 which we are going to model. More detailed analysis with be done along with the simulation waveform.

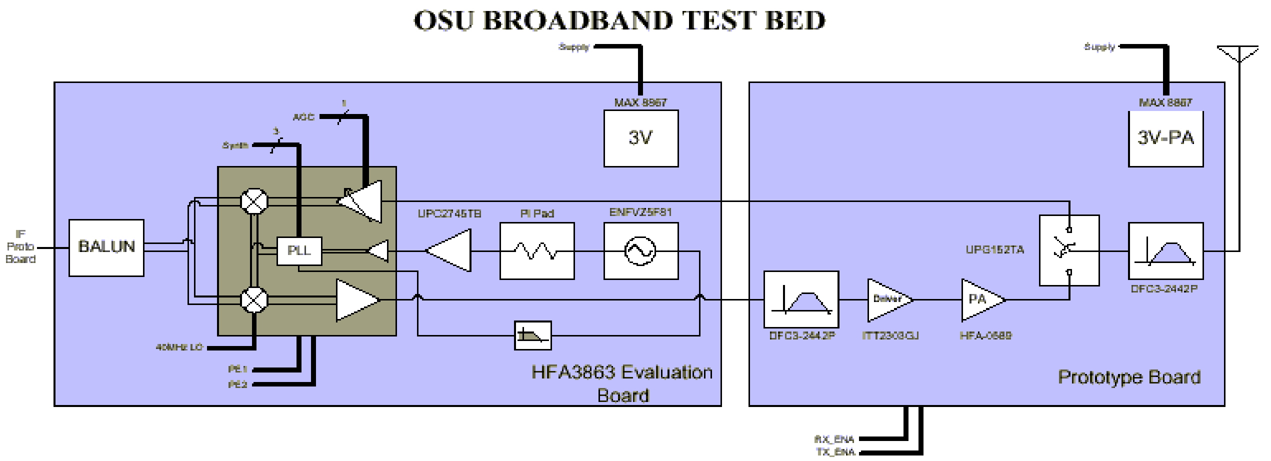


Fig.3.1 Rice Broadband Testbed RF Front end

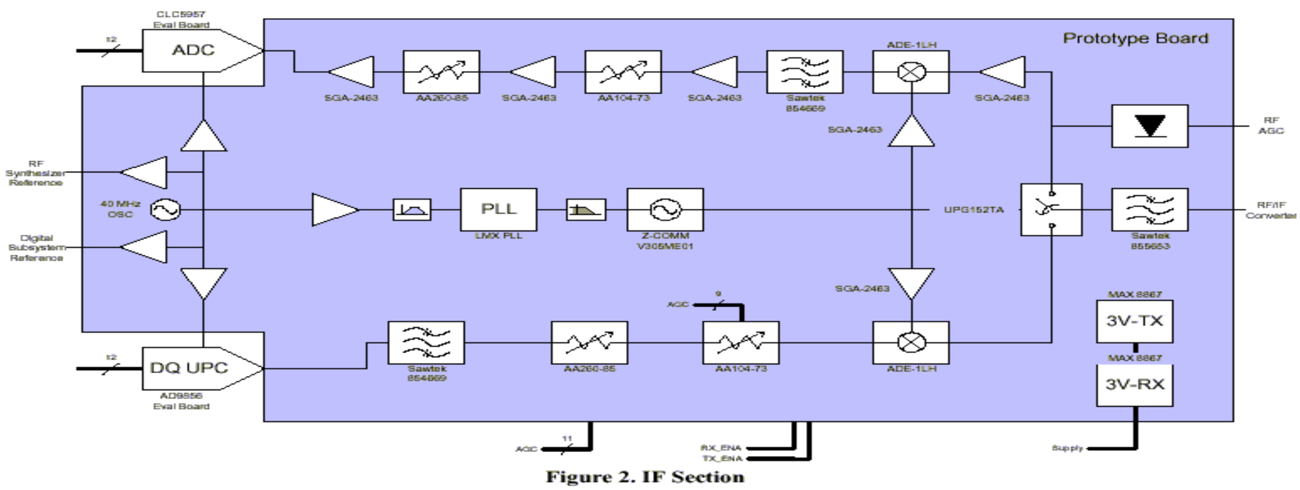


Fig.3.2 Welkin System IF board

The goal of this system is to provide broadband testbed and support evaluation of CDMA user identification algorithms at 2.4 GHz. The system consists of three separate boards. It can interface directly with high speed ADC and DAC at 70 MHz IF both for transmitter and receiver. It is also designed to be a universal platform for base stations, mobiles and interference. In the transmitter chain, an ***AD9856*** DAC/upconverter is recommended to interface with the DSP baseband board. In the IF(Intermediate Frequency) section, the signal first passes through two sets of adjustable attenuators and an AA260-85 amplifier. A SAW bandpass filter with 17 MHz bandwidth and 70 MHz center frequency is used as channel selecting filter. Then via a passive mixer, the IF is upconverted to IF2 at 374Mhz. An ***HFA3683*** IF/RF converter evaluation board from ***Intersil*** is used to upconvert the IF to RF, which is ranged from 2.4-2.484 GHz. Then the signal is power amplified and prefiltered by a ***DFC3-2442P*** filter. The receiver multiplexes the antenna with transmitter through a TDD mode. ***UPG152TAs*** are used to as TDD switch both in the RF section and IF module. The front-end filter DFC3-2442P serves as a band filter to reject interferers outside the 2.4 GHz ISM band. The received signal then comes to the RF/IF conversion evaluation board. The LNA is integrated in the HFA3683 RF/IF converter. This chip has same local oscillator for both transmitter and receiver. The LNA is controlled by 1bit from the baseband to guarantee a wide dynamic range input. In some design, even an off-chip LNA may be needed to provide adequate gain for very weak signal. The TX/RX switch is also controlled by the baseband and typically it is required to be less than 2 μs .

A BALUN is a structure that interconnects balanced and unbalanced transmission lines (BALUN is a contraction of the words balanced and unbalanced). One terminal of a balun's input port is grounded; both output terminals are ungrounded. Ideally, the outputs are "floating": the voltage between either and ground is undefined (just as the voltage between ground and the wires of a balanced, ungrounded transmission line are undefined).

The IF1 in receiver is also set to be 374 MHZ after the down-conversion. The ENFVZ5F81 is a VCO (voltage controlled oscillator) used to generate the local oscillator frequency. This synthesizer in HFA3683 is programmable. In the IF module, the signal from RF module first passes through a ***Sawteck 855653*** filter at 374MHz. To save the cost of design, this saw filter is shared between transmitter and receiver. ADE-1LH is a passive mixer with low insertion loss.

After the signal passes through the IF section, an ADC (recommended as ***CLC5957***) is used to downsample the signal with a 40MHz sampling rate. Then the 12-bit signal is fed into the DSP baseband, which in the current project, is a ***Sundance*** DSP board.

Clearly it is a superheterodyne architecture. A detailed comparison of various transceiver architectures can be found in [16]. While the design considerations will be discussed in section 6.

4. SOFTWARE MODELING

4.1 RF Simulation Tools

The lack of simulators for RF and analog simulations adds up the challenge of RF design and modeling. Even though, since there are several different levels of simulators from behavioral level to circuit level, it is essential to make a survey of the capabilities of current simulators and select the correct one.

[33] and [34] made a comprehensive introduction of the RFIC modeling methods. As a user, we don't need to know many details of the implentation of CAD simulators.However we still need to know the requirement of our simulation and the functionality of current simulators.

RF designers must be able to extract the distortion in RF circuits by simulating a design with reasonable turn-around times. This has to do with the actual computing time required for a simualtion job but also addresses the robustness of the software. Equally important, however, is that the results are accurate and hence reliable.

Virtually the most important features of RF circuits have been introduced in section 2 as non-linearity and distortion. This section made a survey of current RF simulators.

Matlab and mathCAD are general-purpose simulators having been used extensively in engineering such as DSP and communication. Although they provide several powerful libraries in DSP and communication, they don't have an RF library currently. There is a baseband equivalent simulation of RF system. The way is to basically treat all RF signals as Fourier series expansion with time-varying coefficients and then substitute these Fourier series expansions into the transfer functions for the various RF building blocks. By pre-computing the relationship between the time-varying coefficients, the dependence on the carrier frequency can be eliminated. This method is just like the envelope simulation technique used in some RF circuit simulators (like ADS). More information on envelope simulation can be found in papers written by Ken Kundert [34]. However, since this method does not take the effect of high carrier frequency in RF interface and it also doesn't reflect the distortion of the RF circuits, it is not accurate for simulation of system based on true components.

SPICE is a circuit level RF simulator. [35] analyzed the capability of this simulator and some other similar ones. Conventional SPICE-like simulators are not sufficient: transient simulation of RF circuits suffers from excessive CPU times because they have to deal with the absolute bandwidth of the signals and will therefore only be used when no alternatives are available (e.g. full non-linear noise simulation including time domain transient noise sources). AC analysis can easily deal with the high bandwidths but does neither take into account non-linearity nor frequency shifts.

SPW (Signal Processing Workstation) and SpectraRF from Cadence are powerful simulators for RF simulation. **Advanced Design System (ADS)** from Agilent's EEsof also provides a simulation environment suited to mixed DSP/RF simulation. The ability to combine a DSP behavioral simulator in a co-simulation environment with a time-domain non-linear circuit simulator in the complex envelope domain increases utility and improves accuracy. Complex signals such as OFDM and Coded OFDM can be created, and their effects on analog RF hardware performance can be observed, including the reduction in adjacent channel leakage power when coding is used. With ADS, you have access to a wide range of analog, DSP, and RF behavioral models in a user-friendly integrated design environment. It also provides a variety of RF, DSP, system, and RFIC design and simulation tools such **Agilent Ptolemmy**, **Circuit Envelope, SPICE**, and links to MATLAB.
Generally speaking, these workstation-based simulators have a powerful functionality, while the cost and requirement for platform is also proportionally high.

In selection of the simulator, we would prefer to the following capabilities:
1. PC-based simulator with relatively low cost;
2. Take the non-linearity effects of RF circuits into consideration so that it is distortion true;

3. Should support baseband DSP schemes;
4. A flexible interface with other platforms such as DSP, Matlab and simulink for a multi-domain simulation;
5. Parameters and architectures configurable for flexible change of the schemes in a testbed;

Fortunately, **SystemView** from Elanix seems to satisfy all of these requirements. It has a Simulink like functionality for those people familiar with baseband simulation easy to adjust to a new area. It provides simulation of analog components such as SAW filters in RF system and allows modeling of non-linearity of real components such as IP3, IP2, 1dB compression etc. Extended options make it possible to interface with Matlab, Simulink and even TI's code composer for real-time simulation through ***RTDX*** (real-time data exchange). In the following part, modeling of the Welkin RF interface will be described in detail.

4.2 Frequency planning

The first problem encountered in using SystemView is to define the system time and sampling rate. Since we are simulating the analog signal actually in a digital computer, we need to handle all the signals in the system sampled while keeping in mind where the digital part or analog part is.
The main specifications used in the true system are summarized in the following table:

IF1	70 MHz
IF2	374 MHz
RF Range	2.4-2.842 G Hz
Sampling Rate at ADC	40 MHz
Data Bandwidth	17MHz (max)
Symbol Rate	1 MHz(max)
Multi-Access	DSSS(currently), FHSS(future)
Spreading Code	Gold codes, PN codes, Barker Code(WLAN)
Spreading Gain	length 7,15,31 for Gold, 11,13,15 for Barker

Tab.4.1. Technical Specifications of the Welkin System (1)

In order to simulate the system directly, the sampling rate must be high enough to accommodate the carrier frequency f_c. A value of $f_s = (3->5) f_c$ is reasonable. However, the data rate R is usually several orders of magnitude less than f_c. This means that it takes a large number of system samples to process one data bit. This in turn drives the run time of the simulation to extremely large values if it desires to process many data symbol bits for a BER (bit error rate) run. For example, in our W-LAN system, if a symbol rate of 1Msps and a lowest carrier frequency is 2.4G Hz, there are ($N = 4 * 2.4 * 10^9 / (1e+6) = 9{,}600$ system samples per symbol. If the goal is to simulate a BER to the order of $1.0e^{-3}$, then at least $1e^{+4}$ symbols should be processed (for BPSK). The total number of points in the simulation is then a prohibitive $9.6e^{+7}$ number of points.

(1). Frequency Re-planning One solution to this problem is to use a carrier frequency less than the actual carrier frequency for the purpose of the simulation. As long as the filter bandwidths and power levels are maintained, the simulation result will be the same in either case. There is no hard and fast rule as to how far the carrier can be reduced. However to do a frequency re-planning, we need to pay attention to the compatibility to potential bands in the standard. For example, in WLAN 802.11 there are 3 separate bands for frequency reuse, each with 22 MHz bandwidth. The new frequency planning should be able to accommodate the requirement of new simulation extensions.

(2). Baseband Equivalent Processing A second solution is to eliminate the RF altogether. This is known as baseband equivalent processing mentioned earlier. The objective is to develop an analytical expression which represents the process of modulating the data on a carrier, processing this RF signal, and finally demodulating the signal back to baseband. In this way, the RF frequency is completely eliminated from the simulation. The simulation sampling rate need to be only high enough to accommodate the bandwidth of the information (baseband) signal. Clearly it is several orders of magnitude less than that required if the RF frequency was directly simulated. However, this method does not reflect the effects of real RF components and are not accurate.

In this simulation, the RF output carrier is scaled to 442 MHz instead of the original 2.442 GHz. Thus the ISM band can be mapped from range *2.4 GHz ->2.484 GHz* to *400 MHz -> 484MHz*, with the center frequency of 442 MHz. This lower frequency RF is produced by changing the LO frequencies of the transmitter's IF-RF up converter, and the receiver's RF-to-IF up down converter, from *2.068 GHz to 68 MHz.*

Since the maximum rate used in this system is 442 MHz, if we uses 5 times, 5*0.442 = 2.210G Hz. To get accurate amplitude readings, the number of samples, and sample rate parameters should be set numbers that are " powers of 2" to avoid zero padding of FFT operation. So finally we set the system rate at *3.2768 GHz*= $2^{15} * 10^{5}$.

The sampling rate and system time can be set as Fig.4.1. With this setting, the frequency resolution is 50Hz with 65536 samples.

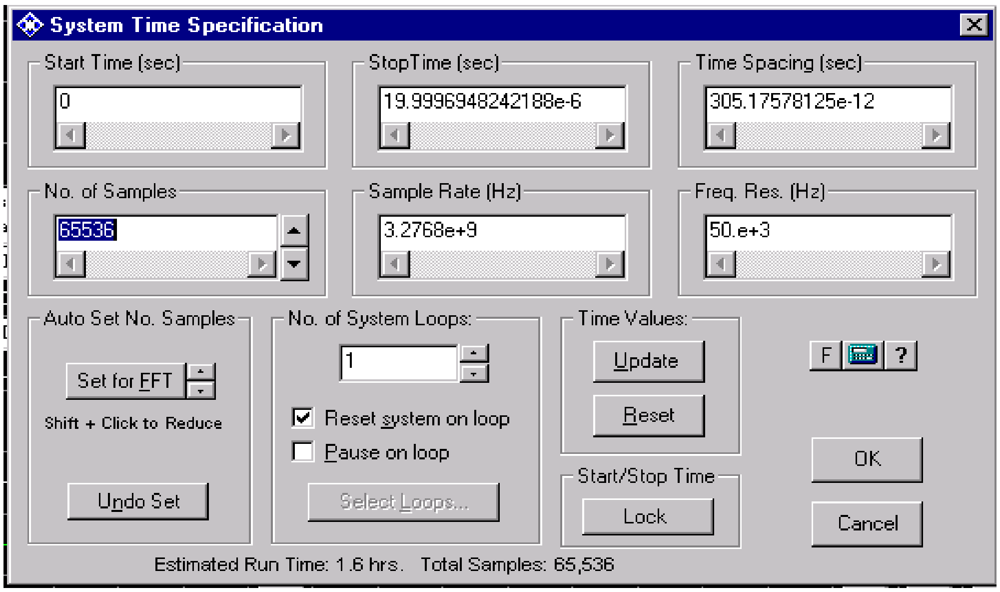


Fig.4.1 System Timer Configuration

4.3 **Multi-rate Processing**

However it is still not enough by just setting this single scaled system rate. In the low-frequency band, this sampling rate is still too high. For example, to design the 70 MHz Sawtek 854669 filter with 17MHz bandwidth, the relative frequency of 0.002 to the system rate is needed. Up to **6,000 taps** should be used for accurate cut-off effect of FIR filters. This may take too long to design filter and also introduce too much group delay in the simulation. To solve this problem, we combine the tokens in the sampler/hold library flexibly to down-sample or up-sample in different stage, thus provide a multi-rate processing in the system. It should be pointed here that there are several different samplers with different function. A good knowledge of the library and also the actual feature of the analog/digital signal are important in selecting the correct tokens. Actual situation is judged case by case.

4.4 Cascaded System Architecture

A module partitioning is essential to the system division and reuse. In this design, the system is defined as the following subsystem: (1).Baseband transmitter;(2).RF transmitter;(3).Channel;(4).RF receiver;(5).Baseband receiver;(6).BER measure system as shown in Fig.4.2.(Appendix). To compare with the scheme without RF, a corresponding baseband link is also used here at the bottom of the system. The following sections will carry out a cascaded analysis of the system based on the design and also the signal of each stage both in time domain and frequency domain.

4.4.1 Baseband Transmitter

Shown in Fig.4.3 is the baseband transmitter. This is the scheme expected to run in the Sundance DSP board for transmitter. Here two separate PN generators are used to generate the random symbol stream for both I/Q (In-phase and Quadrature phase). For simplicity, the level is set to 2 and the output is the antipodal signaling S {+1, -1} which implies a QPSK scheme. Then an XOR operator is applied to do the differential encoder. The delay of the feedback of the encoder is the length of one symbol: *1e-6* second. The symbol then passes through the Matlab token to do spectrum spreading. The rule for the differential encoding is that if the present input bit is a ONE, then the output state of the encoder does not change, and vice versa. The XOR operation is formulated as:

$$Dout[(m+1)Tb] = \overline{Din(mTb) \oplus Dout(mTb)}. \qquad (6)$$

The DPSK signal received is decoded by the reverse operation, as depicted in Fig.4.4 baseband receiver. The advantage of DPSK is the possibility of non-coherent detection without knowing the time origin because the information lies in the phase "change".

Direct Sequence Spread Spectrum

That spread-spectrum communications offer greater user capacity than narrowband techniques in a given piece of wireless spectrum is well known to the community. Much has been written on this subject [31]. Conventional narrow band wireless communications require a careful discipline enforced by FCC or other government agencies while issuing licenses so as to prevent use of the same frequency by nearby operators. However for spread spectrum use, the FCC has allocated certain unlicensed bands in the United States, referred to as the instrumentation, scientific, and medical (**ISM**) bands. The use is only required to spread spectrum by a minimum amount, and not to exceed an upper limit on transmitted power.

Basically there are two different methods to spread the spectrum of a signal: by direct sequence modulation **(DSSS)** or by frequency hopping **(FHSS)** (hybrid mode can be viewed as the extension of these two). Direct sequence is conceptually the simpler, as well as the more straightforward to implement. Each data bit *{+1, -1}* at the transmitter multiplies a prescribed sequence of bits, or chips as they are called. The chip sequence is selected for very low auto correlation, and is often referred to as pseudo-noise (PN) sequence. Each user is assigned a unique shifted version of some long PN sequence with very low cross-correlation with other user sequences. The receiver, after an initial acquisition search to align itself with the start of the PN sequence, correlates the incoming sequence with the pattern it knows to be its own. On detection of a correlation peak, the sign of the peak signals indicates the source data bit. The longer the PN sequence for each bit, the greater the spreading gain, and the more reliable the detection.

The characteristics of spread spectrum can be summarized briefly here: (1) Low power spectral density so the information signal looks like noise to eavesdroppers or other radios; (2) High immunity to jamming and interference; (3) High resolution ranging; (4). Possibility for code division multiple access (CDMA).

In this testbed several spreading codes will be supported. These include *PN random long code, Gold Code, Barker Code or Walsh Code.* The Gold code is used in previous W-CDMA testbed for its better periodic cross-correlation properties than m-sequences. Barker code is recommended by IEEE 802.11 WLAN standard. Although SystemView provides a token to generate gold code, for flexible extension to other codes, a matlab custom block is used to spread the spectrum with different spreading code and spreading gain. The code type is set as a parameter. Since the bandwidth is 17 MHz and gold code has length {7,15,31}, for a 1Msps symbol rate, length 7 is closest to the bandwidth. If the symbol rate is ***R***, the spreading gain is ***Gs***, then after spreading, the bandwidth is ***W=R.Gs***. The codes are read from predefined files with a Matlab interface, so the symbol is first sampled at the symbol rate as the input of the Matlab token.

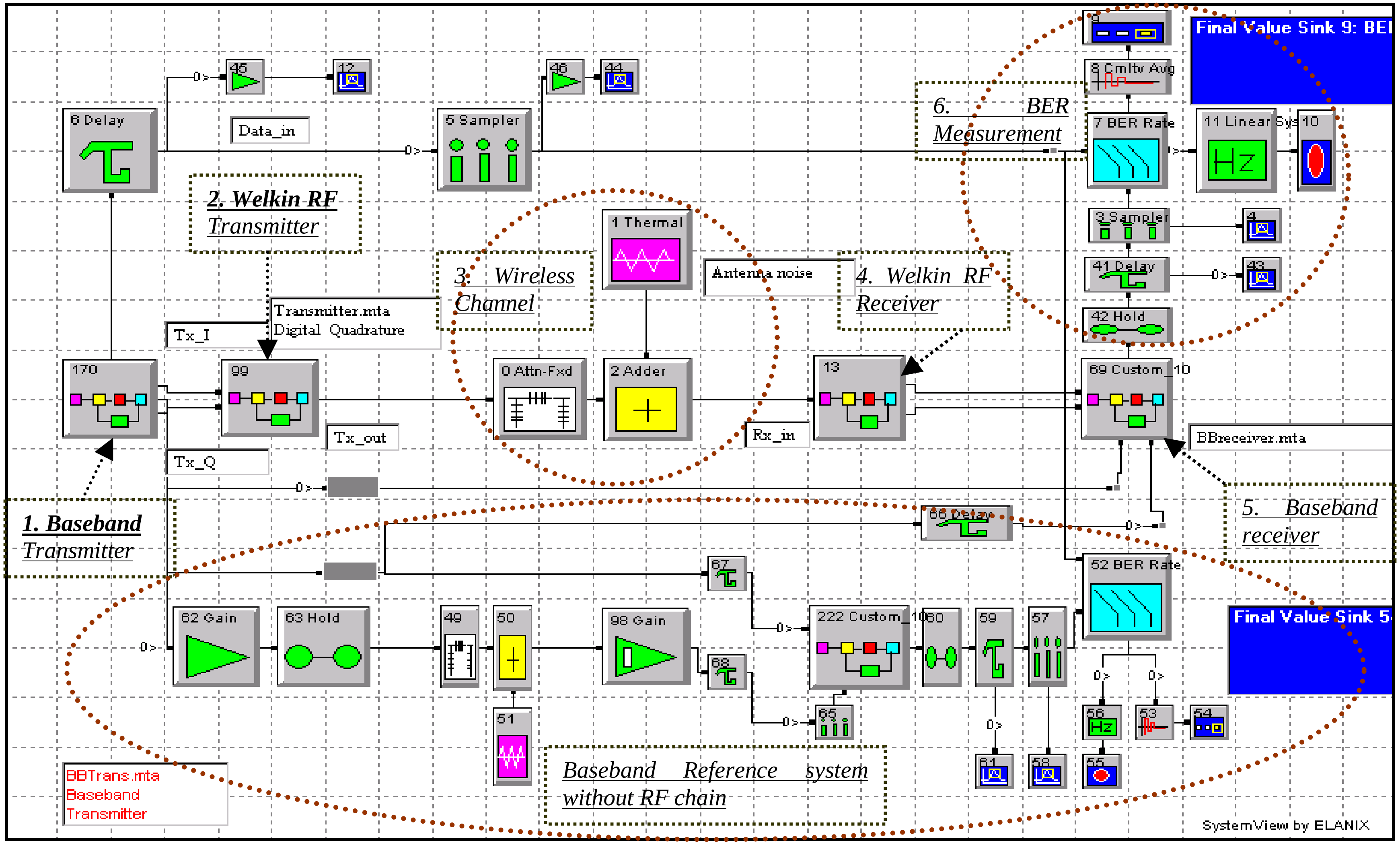


Fig.4.2 Complete System Blocks of W-CDMA with Welkin RF System

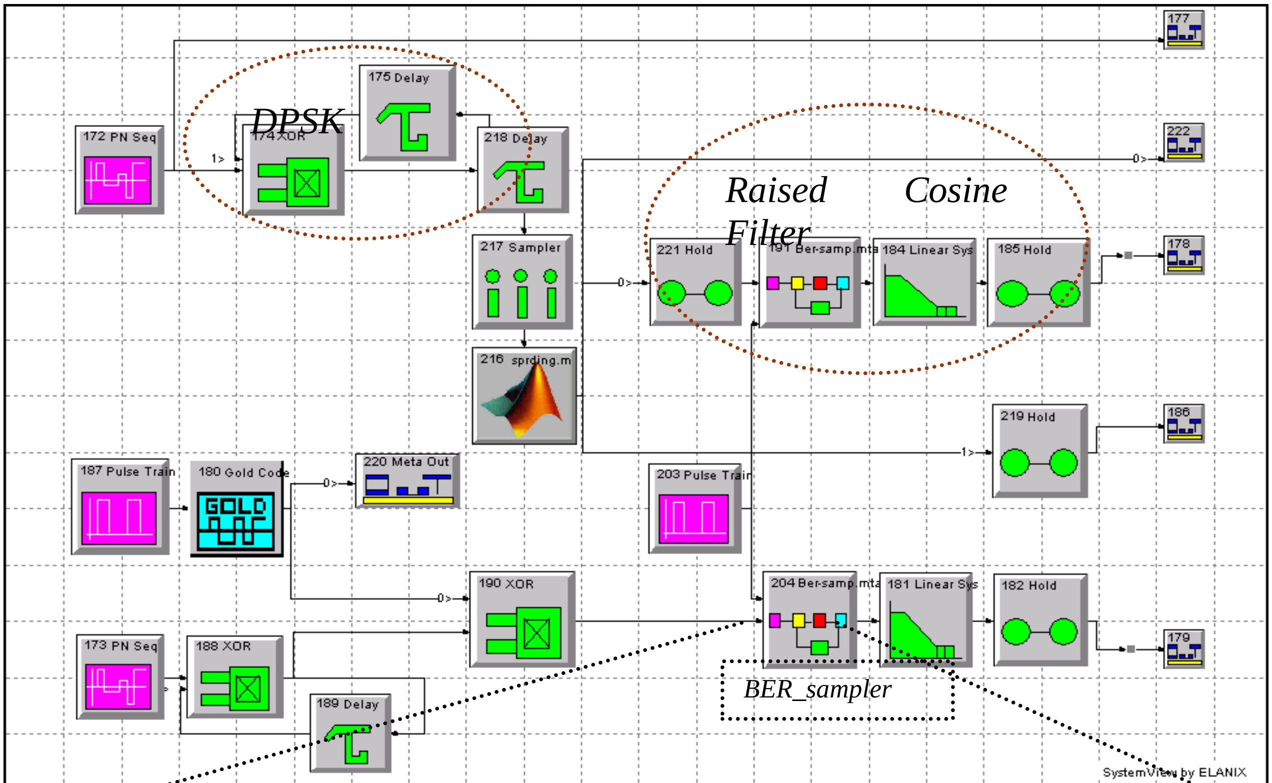


Fig.4.3 W-CDMA Baseband Transmitter

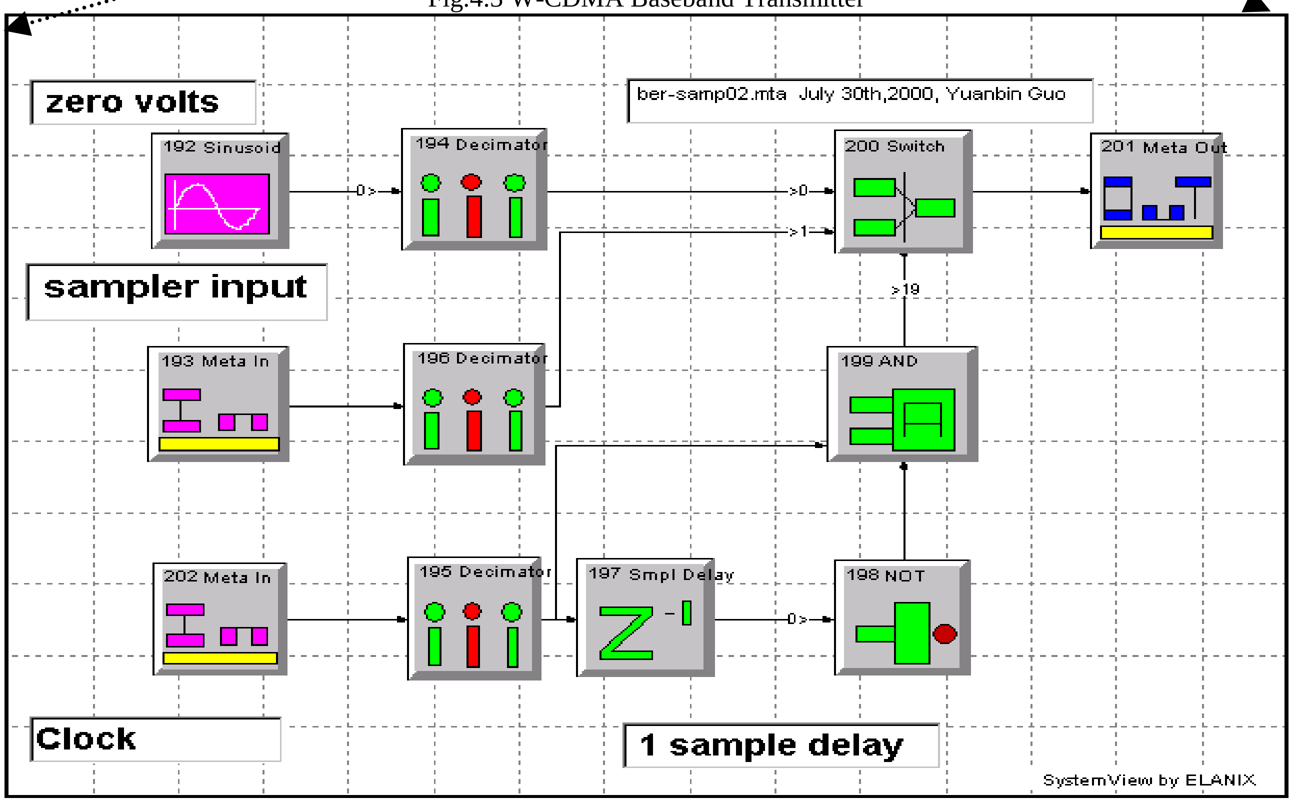


Fig. 4.4 BER-sampler for pulse sampling of raised-cosine filter

Spreading can be done with a pair of XOR operations in the transmitter and receiver for *{0,1}* bit streams. It has also been shown that the operation of multiplying is equivalent to the operation of modulo-2 addition for spreading for signaling {+1,-1}. So in this simulation, the spreading is done by $\sum_n \sum_m b_n \times c_{m-n*Gs}$ where b_n is the bit and C is the spreading code.

PN code can be generated with shift register. Gold code can be generated from a pair of preferred sequences, say **a** = $[a_1 a_2 ... a_n]$ and **b**= $[b_1 b_2 ... b_n]$ by taking the modulo-2 sum of **a** with the *n* cyclically shifted versions of **b** or vice versa [3]. Barker code are named after Ronald H. Barker who first used them as frame sync markers in a matched filter that used digital signals [42]. They are also known to possess good aperiodical correlation properties, which means that due to the non-repetitive behavior of the code a matched filter correlator can easily identify the location of a Barker code in a sequence of bits. The same properties that make Barker codes good frame sync markers also make them good PN codes for spreading and despreading DS signals. Table 4.1.contains the complete listing of all known Barker codes [43].

Code Length	Barker Sequence
1	+
2	++ or +-
3	++-
4	+++- or ++-+
5	+++-+
7	+++--+-
11	+++---+--+-
13	+++++--++-+-+

Tab. 4.2 Listing of Known Barker Codes

The list of known Barker codes is limited to eight sequences. Due to their relatively short length, Barker codes are convenient when fast PN code synchronization is a requirement.

Baseband Pulse Shaping for Improved Spectral Efficiency

In our simulation, ***NRZ*** (not return to zero) pulse shape is commonly used. In this format, a logical one is one level and a logical 0 is the other. While using antipodal signaling, {1, –1} are used. The mathematical description of the NRZ waveform is given by the equation below.

$$d(t) = \sum_{k=0} c_k \, p(t - kT) \tag{7}$$

$$where \quad \begin{cases} c_k \in \{+1, -1\} \\ p(t) = 1 \quad 0 \le t \le T \\ p(t) = 0 \quad otherwise \end{cases}$$

It is instructive to rewrite the above equation into a slightly more complicated but more useful form,

$$d(t) = \sum_{k=0} c_k \delta(t - kT) \, p(t) \tag{8}$$

Of course *p(t)* can be chosen which has an arbitrarily narrow spectral occupancy. However, the filter output after driving it with the data impulse washes everything, and thus it is generally impossible to separate out the data after the filter. This is the concept known as inter symbol interference (**ISI**).

Nyquist proposed that the shape of each data pulse be such that the signal be band limited and yet there be no **ISI** (Intersymbol Interference) due to preceding or following pulses at each sampling (or decision making) instant. He proposed three different methods for doing this. Filters, which produce pulse shapes with no ISI at each sampling instant, are referred to as Nyquist I type filters. Nyquist II filters employ filters whose pulse shape is such that pulses can be sent at a rate of 2 f_b within a bandwidth of f_b and still unambiguously interpreted. Nyquist III filters have pulse shapes such that the total area in all pulse not at *t=0* are zero.
In this report we only studied the raised cosine filter in the digital form. The unique of the raised cosine filter is that the nulls of the ringing occur at multiples the input data rate. Because of the position of the nulls, there is no additive interference due to previous symbols. A system using this type of filter produce zero ISI, thus giving more margin to the BER requirement by the noise introduced by the channel. When the filter is implemented in digital form, a general-purpose DSP processor like TI's C6000 can be used.
Raised Cosine Filter is defined as:

$$P(f)=\begin{cases} T_s & 0<|f|<\dfrac{1-\alpha}{2T_s} \\ T_s[1+\cos\dfrac{\pi T_s}{\alpha}(|f|-\dfrac{1-\alpha}{2T_s}] & \dfrac{1-\alpha}{2T_s}|f|<\dfrac{1+\alpha}{2T_s} \\ 0 & |f|>\dfrac{1+\alpha}{2T_s} \end{cases} \tag{9}$$

Here α is the roll-off factor. The pulse shape is formulated as,

$$p(t)=\frac{\sin(\pi t/T_s)}{\pi t/T_s}\frac{\cos(\pi\alpha t/T_s)}{1-4\alpha^2t^2/T_s} \tag{10}$$

When using raised cosine filter to do pulse shaping, a new complication appears. The system sampling rate is ***Fs=3.7268 GHz***, which is too high for the baseband signal operation. To use the raised cosine filter, the input rate to the filter needs to be reduced from 3.7268GHz to 104.2MHz and the output sampling rate should be brought back to the system rate for further operation.
The first task is achieved by the metasystem *ber_samp.mta* shown in Fig.4.4. The three decimate-by-32 tokens change the sampling rate to 102.4MHz. The clock in the meta system is set to the same frequency as the desired data rate (7 MHz for length 7 Gold code) and the phase is set to 180 degrees. In the metasystem, a digital differentiator makes up a delay. The switch put out zeros at the new rate of *102.4e+6* samples/sec between samples. The second task of bringing the output of the filter back up to the system rate is done using a Hold token set to the Hold-last-sample mode. The output of the Hold token is always at the system rate, in this case 3.2768 e+9 samples/sec. Fig.4.5.shows the design of raised cosine filter with roll-off factor at 0.25.With the input rate at 102.4 MHz, the filter needs 85 taps. There is a gain in the hold token. The gain is computed as ***104.2MHz/7MHz=14.628*** to make the input sampled data points (with amplitude of +1/-1 volts) coincide with the filter's output waveform.

The operation of baseband signals is shown in Fig.4.6. The rectangle waveform with amplitude 1.5 is the original symbol bit before differential encoder (marked as signal 1). The rectangle waveform with amplitude of 1.25 is Gold-7 spreading code (here it is {-1,-1,1,-1,1,1,1} and marked as 2). This code is repeated periodically for each bit length. The rectangle waveform with amplitude 1 is the spreaded chip stream (signal 3). To view the chip samples they are plotted as a pulse train as the output of subsystem BER_sampler.mta (signal 4). This pulse train is also the input of the raised cosine filter since the pulse shape is just the pulse response of the raised cosine filter. At the output of raised cosine filter there is loss of amplitude (signal 5). The gain in hold token is used to recover the gain and the resulted waveform (signal 6) is the one coincides with the input pulse of raised cosine filter. It looks like a stair after the hold token. This will be re-sampled at the rate of the upconverter inside DDS (Direct Digital

Synthesizer). Shown in Fig.4.7. are the corresponding spectra. From the figure we can see clearly that the original data has a 1MHz bandwidth and the spreaded data has a bandwidth of 7MHz. When it is pulse-shaped, the spectrum is concentrated to 5.5 MHz.

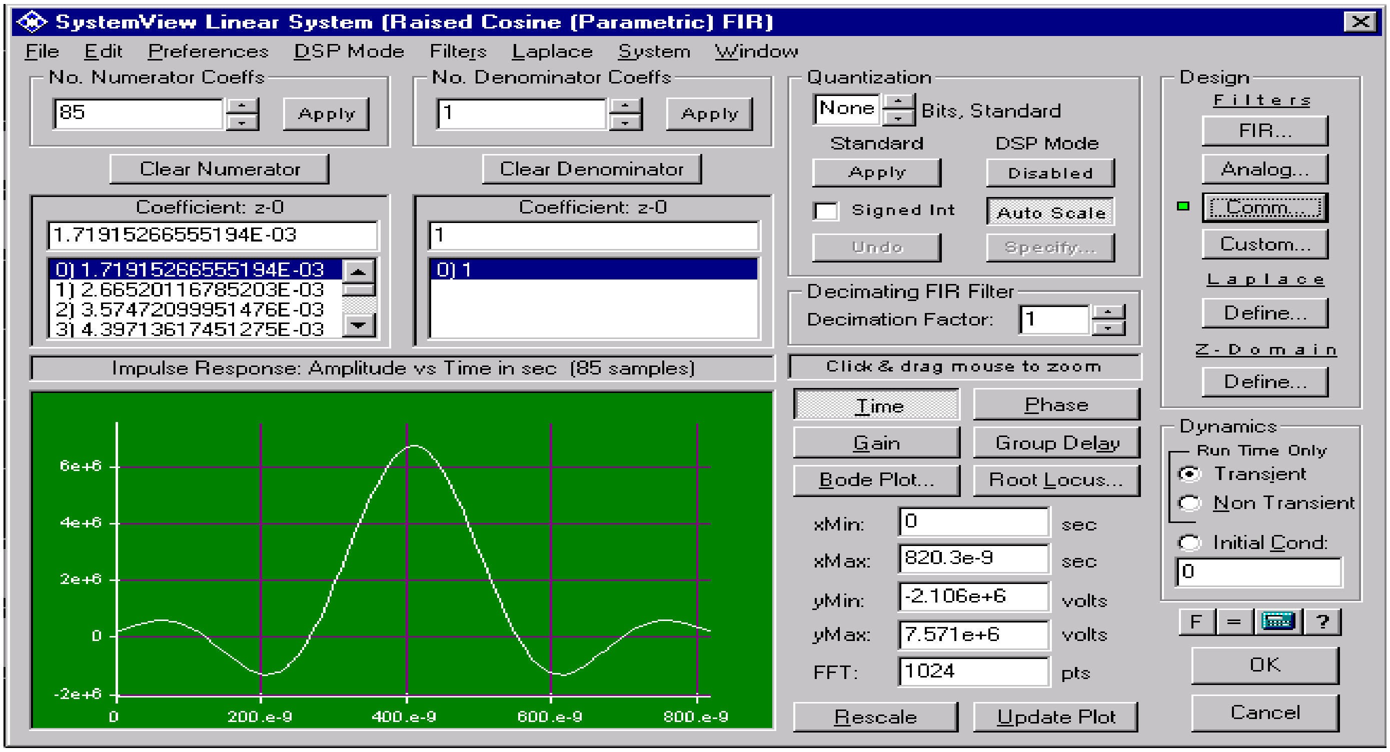


Fig.4.5 Design of Raised Cosine Filter

A convenient way of visualizing ISI qualitatively is the so-called eye diagram. In the eye diagram, the output signal is "folded" back onto itself modulo ***T*** sec. An oscilloscope with a trace time of T seconds and set in a persistence mode will generate the eye diagram. Fig.4.8 shows an "eye" diagram of a raised cosine filter. The shape cross over point in the middle is the ideal sampling point. Notice that there is no ISI at the sampling instants. The overall pulse shape is sinusoidal in appearance, suggesting a narrower power spectral density. This is in fact the case. Fig.4.9. shows the unfiltered BPSK and a BPSK signal whose modulation signal has been passed through a raised cosine filter. As a result, the height of the first lobe is down only 13.2 dB from the main peak in the unfiltered signal. This is unacceptable spectrum efficiency for most user applications. As it passes through a raised cosine filter, the height of the first lobe is down to ***35*** dB. This meets the spectral mask requirement of WLAN 802.11 standard: **30dB.**

4.4.2 RF Transmitter

The RF transmitter meta system features a DAC/upconverter, the welkin IF section, RF section and preamplifier. The blocks are shown as in Fig. 4.10.

DAC/upconverter: DDS

The recommended AD9856 features some half-band filters and a direct digital synthesizer (DDS) as well as Inverse Sinc filter (optional) and a 12-bit DAC. This component is modeled by the meta system shown in Fig.4.11. The actual interface with baseband DSP is 12 bits complex data input, then the Data Assembler splits the incoming data word pairs into separate I/Q data streams. Here for simplicity, the inputs are already separated I/Q data. The half band filter has a linear phase response and almost no insertion loss. So there is almost no phase distortion in the passband. According to the specification of AD9856, if the baseband data applied to the AD9856 has been pulse

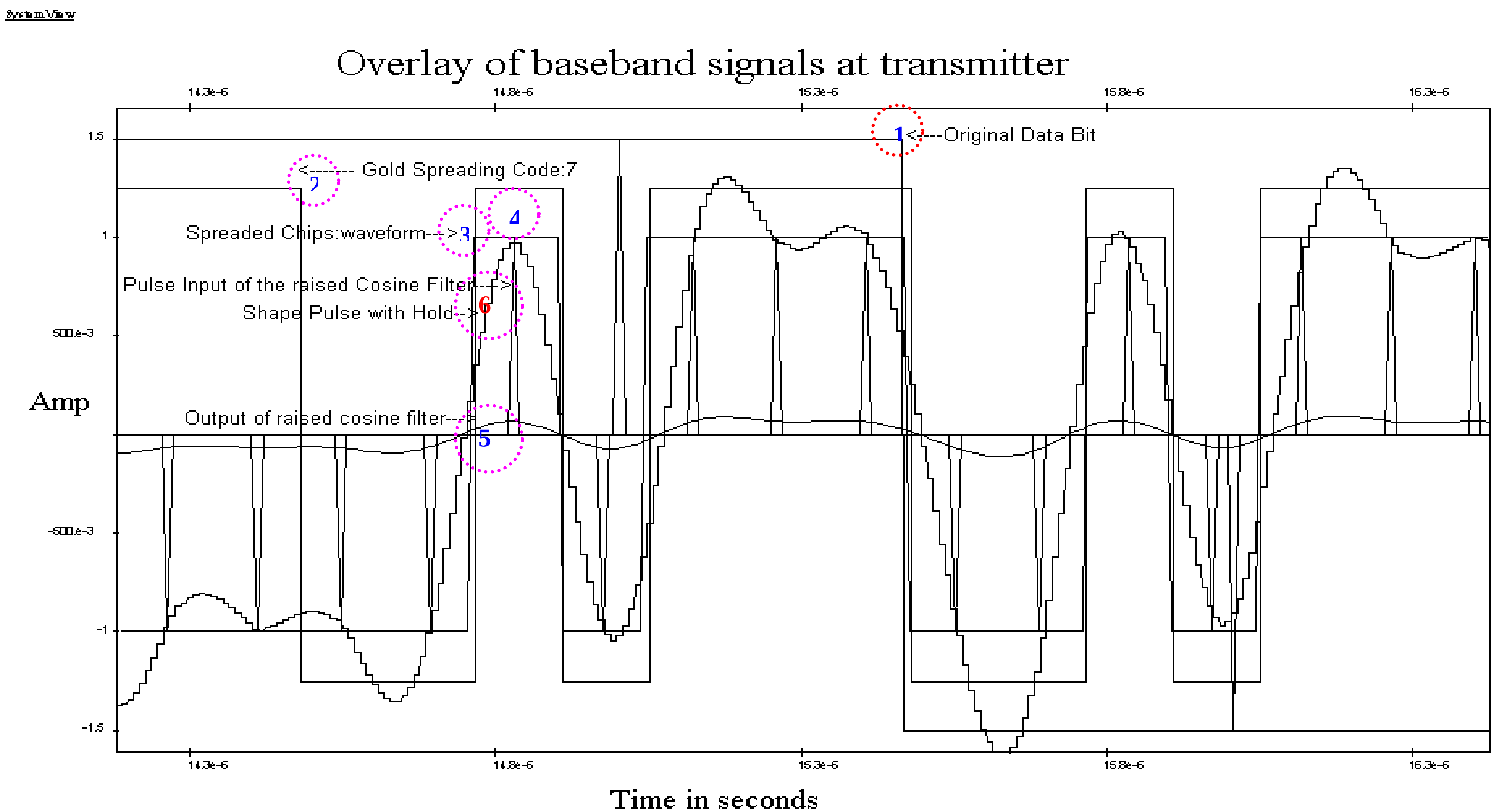


Fig. 4.6 The overlay of baseband signals: Original Data Bit, Gold Code, Spectrum spreaded data

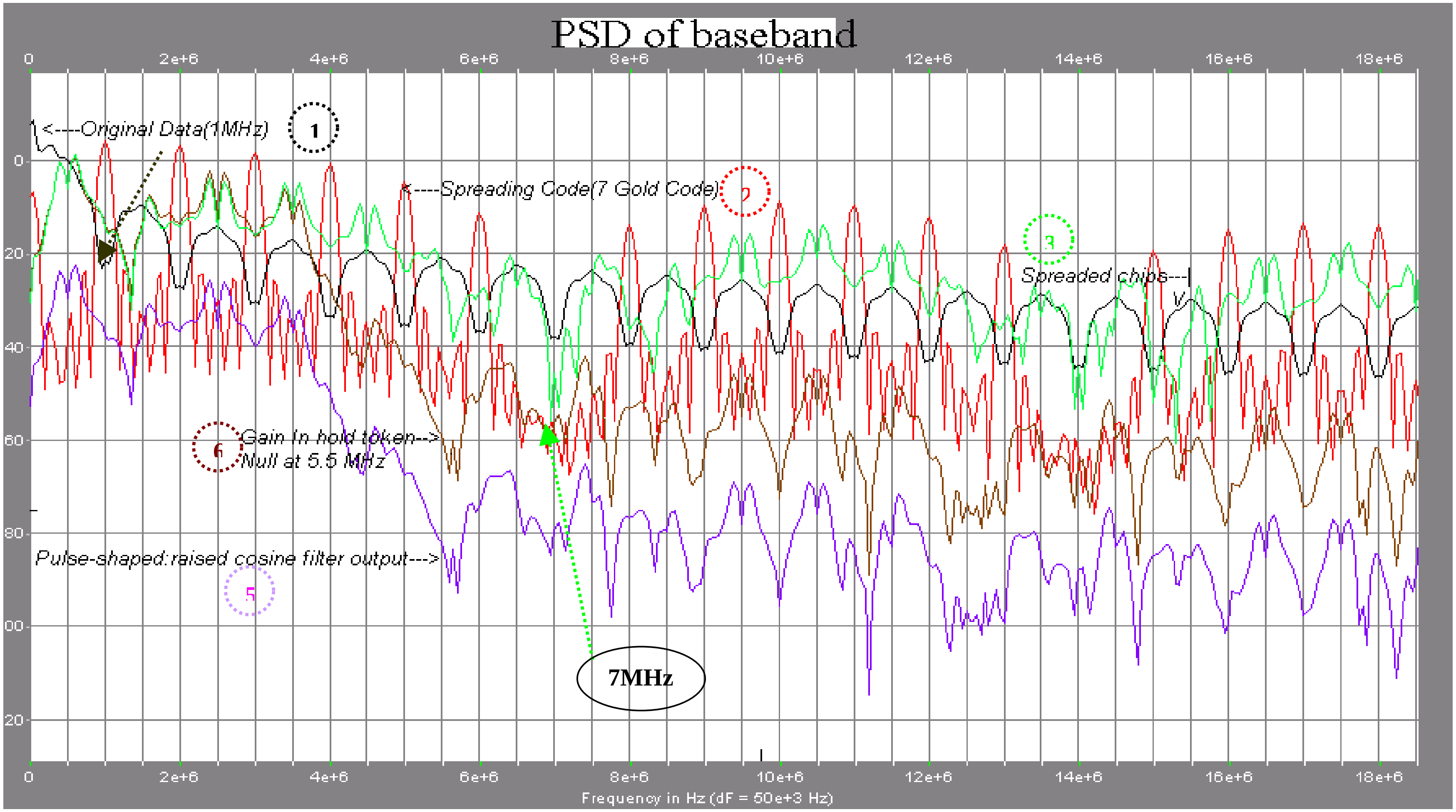


Fig.4.7 corresponding spectrum of Fig.4.6.

shaped, the user must oversample their baseband data by at least a factor of two. A maximum value of roll-off factor 0.8[29] is acceptable. After the half-band filter, the sampling rate is increased by a factor of 4 or 8, depends on the configuration of the third half-band filter in the chip. To reflect this, a hold and a sampler token are combined. Also to reflect the effect of DDS (digital direct synthesizer), a cosine/sine source is sampled at the same rate of data before applied to the two I/Q channel mixers. DAC output spectrum is distorted with DAC-generated signals, this distortion is deterministic and follows the familiar sin(x)/x(or SINC) envelope because of the intrinsic zero-order hold flat top effect. An INVSINC is an option to compensate the spectrum. The local frequency (LO) is set to be 70 MHz. Then a 12-bit quantizer is used to simulate the limit word length effect and a hold-last sample token used to change the sampling frequency to the system rate (analog).

If the I/Q has an input amplitude of {+1,-1}, then the upconverted signal is $\pm\cos\omega_1 t \pm \sin\omega_1 t = \pm\sqrt{2}\cos(\omega_1 t \mp \frac{\pi}{4})$. This means after the upconverter, the signal has been modulated to 70 MHz IF frequency with a phase of $\pm\frac{\pi}{4}$.

It should be noticed that the input signal to the quantizer should be less than the maximum level of quantizer. Otherwise, saturation will appear thus cause a very serious distortion of the signal. The result is reflected in the BER curve as compared later.

IF section

In the transmitter IF section, the signal first passes through a SAW 854669 bandpass filter. SAW (Surface Acoustic Wave) components have many advantages derived from their physical structure. The basic idea is to first convert the electromagnetic wave to an acoustic wave (Fig.4.12). Because the relative high wavelength of acoustic wave to electromagnetic wave, the device can be made very small sized. Then the acoustic is converted back to the electromagnetic signal. Because of the physical effect, SAW filter has such advantages as small-size, linear phase, low shape factor and excellent rejection. The frequency response resembles the finite impulse response design techniques very similar to those used for digital filters. Actually the principal design tools for SAW filter are those used to design FIR filter.

SAW filter is always suffered from a high insertion loss. So the SAW filters simulated here with a FIR filter followed by an attenuator. Because it is a passive component, the noise figure is almost similar to the loss. So the attenuator is set to “noise figure enabled”. The filter used here is shown in Fig. 4.12.1 with the specifications from SAW 854669.

Center Frequency	70 MHz
Insertion Loss at F_0	13.5dB
1 dB Bandwidth	17.55 MHz
3 dB Bandwidth	18.5 MHz
40 dB Bandwidth	23.4 MHz
Passband Ripple	0.7 dB

Tab.4.3 Specification of SAW854669

Following this filter, an AA260-85 is a GaAs IC 5-bit digital attenuator. This attenuator is combined with AA104-73, a 1 bit GaAs IC FET digital attenuator to provide an adjustable attentuation for AGC (automatic gain control) of transmitter. Typical parameters of these two components are:

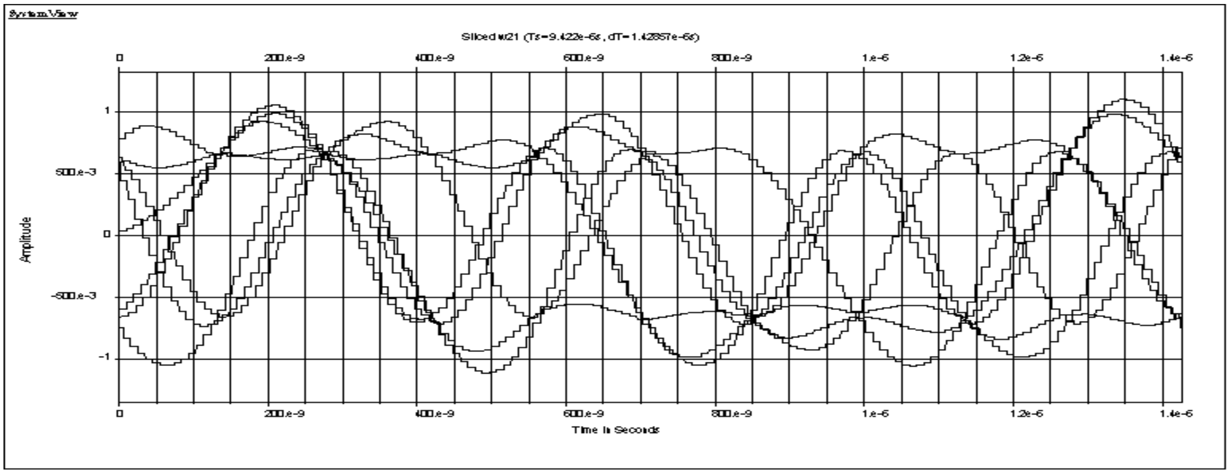


Fig. 4.8 Eye-Diagram of raised cosine filter output and the following flat-topped waveform

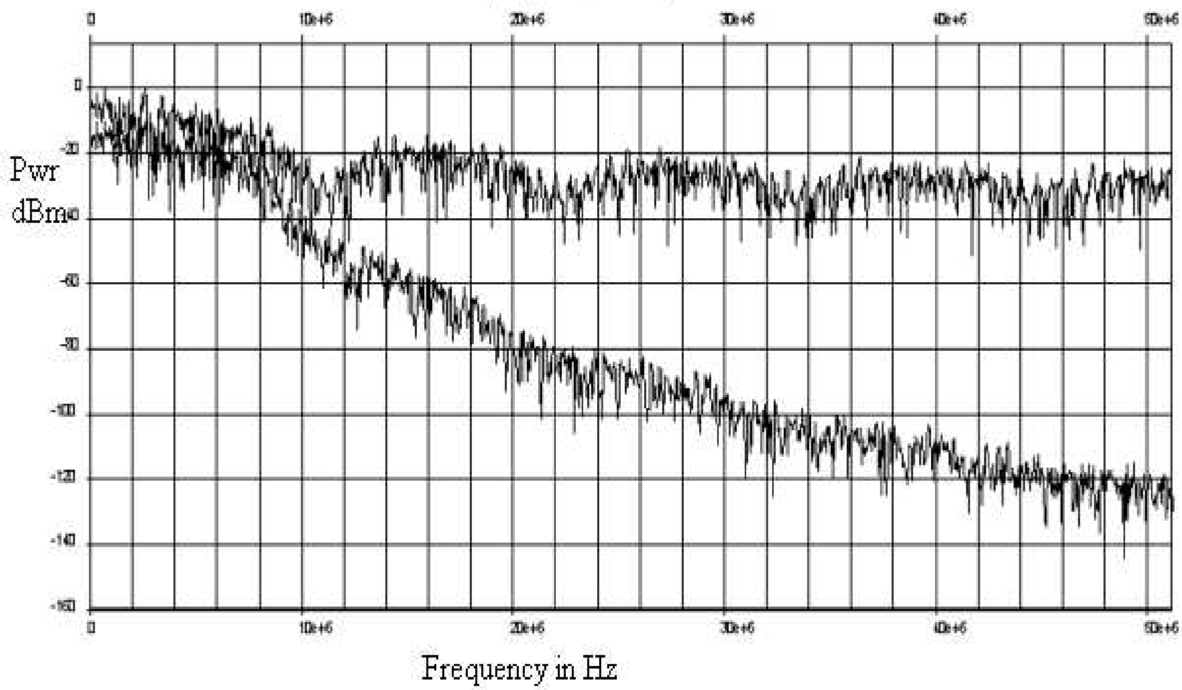


Fig. 4.9 Spectral mask shows that pulse shaping inmproves the spectral efficiency

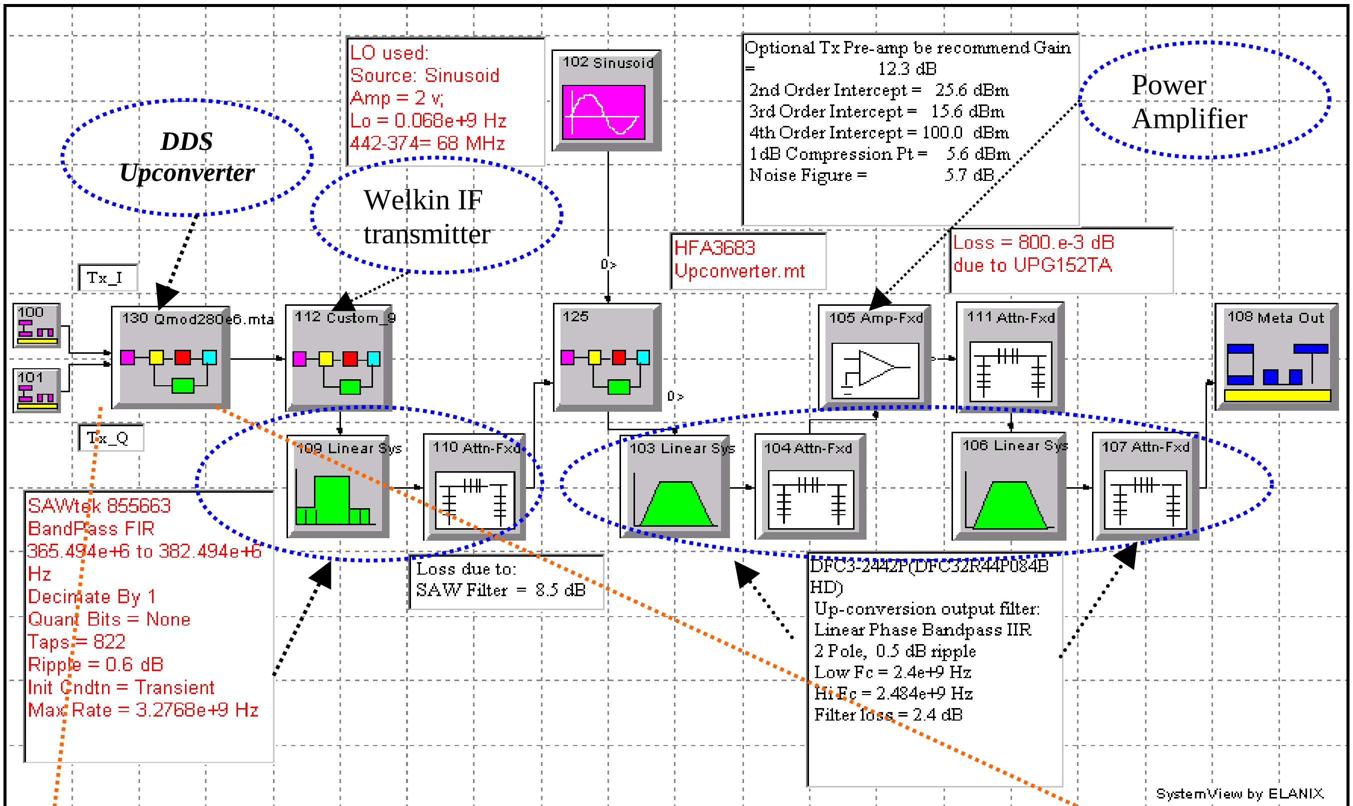


Fig.4.10 Welkin RF transmitter

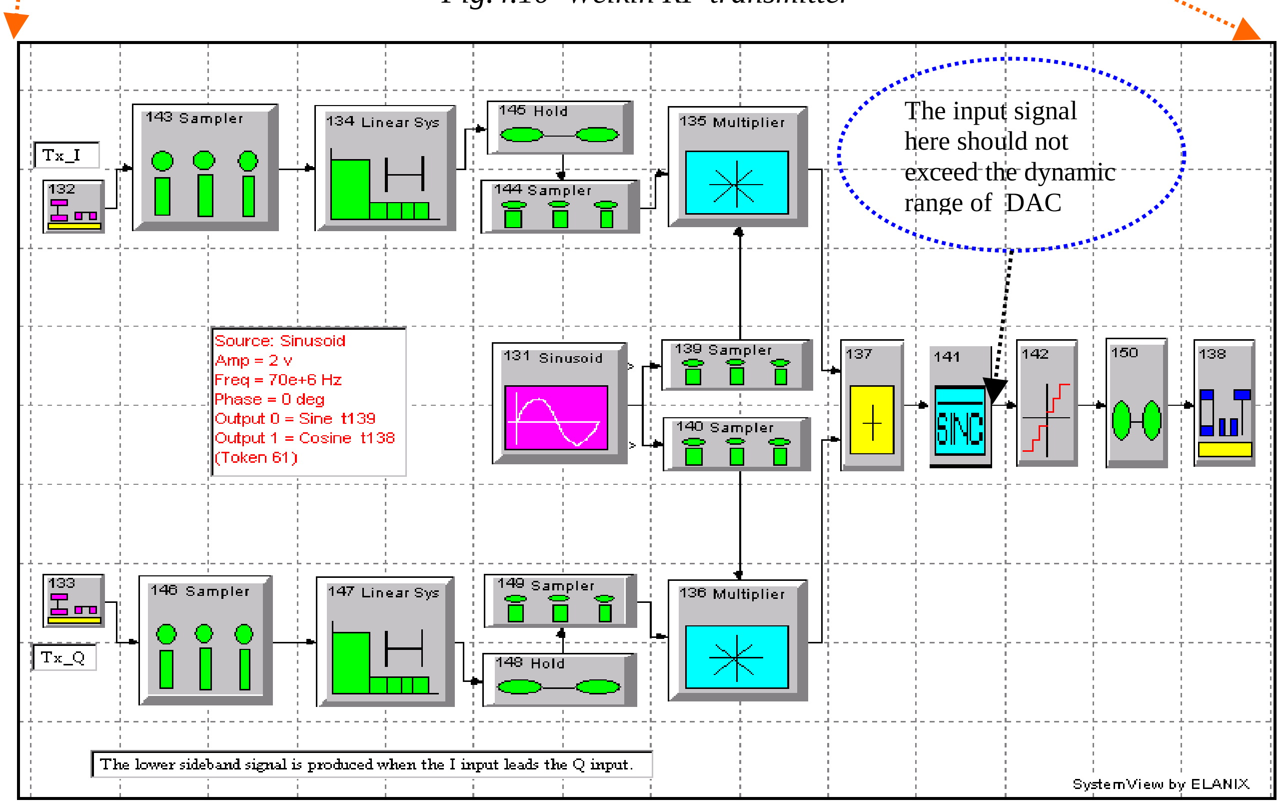


Fig.4.11 ADC/Upconverter with a DDS and 12-bit quantizer

	AA260-85	AA104-73
Bits	5	1
Insertion Loss	1.5dB(DC-0.5 GHz)	0.8dB(DC-1.0GHz)
Attentuation Range	31 dB	32 dB (DC-1.0GHz)
P1dBin	+27dBm	+21dBm
IP3	+45dBm	+41dBm

Tab. 4.4 Specifications of Attenuators

Typically attenuators are required to have a high input 1dB compression point and also a high inter-modulation intercept point 3. The parameters shown above satisfy these requirements. To simulate the corresponding non-linearity effect, a fixed amplifier is followed with corresponding P1dB and IP3 specification.

A passive mixer is used to simulate the ADC-1LH mixer. An SGA-2463 amplifier is used to amplify the LO frequency at 304 MHz. The specifications of ADC-1LH used here is:

Frequency	Conversion Loss	LO-RF Isolation	LO-IF Isolation	IP3
DC-500MHz	5.0 dB	55dB	45dB	15dBm

Tab.4.4 Specifications of ADC-1LH

SGA-2463 is a high performance cascadable 50-ohm amplifier designed for operation at voltages as low as 2.6V. This RFIC uses the latest SiGe HBT (Silicon Germanium Heterostructure Bipolar Transistor) technology and has the following features:

Output IP3	Noise Figure	Output P1dB	Gain
19.7dBm	2.7dB	8.1 dBm	20.3 dB

Tab.4.5 Specifications of SGA-2463

Reviewing the concept of non-linearity and definition of P1dB compression, we hope the RF components work in the linear range. So the input signal should not exceed the input P1dB or the output signal should not exceed output P1dB. Since the local frequency is using SGA-2463 as the amplifier, the output P1dB=8.1dBm. The input P1dB=8.1dBm-20.3dB+1dB=87mV. So guarantee a linear working mode, we used 50 mV local frequency here.

The UPG152TA is a TDD (Time Division Duplex) mode switch for the transmitter/receiver. Its effect is modeled as the attentuator with the same insertion loss of the switch. Return to Fig 4.3, a SAWteck 855653 is applied here after the switch. The parameters are listed below. A FIR + attentuator scheme is also used here.

Center Frequency	Insertion Loss	3dB Bandwidth	Passband Ripple	50dB Rejection
374 MHz	8.5dB	17 MHz	0.6 dB	22MHz

Tab. 4.5 Specifications of SAW 855653

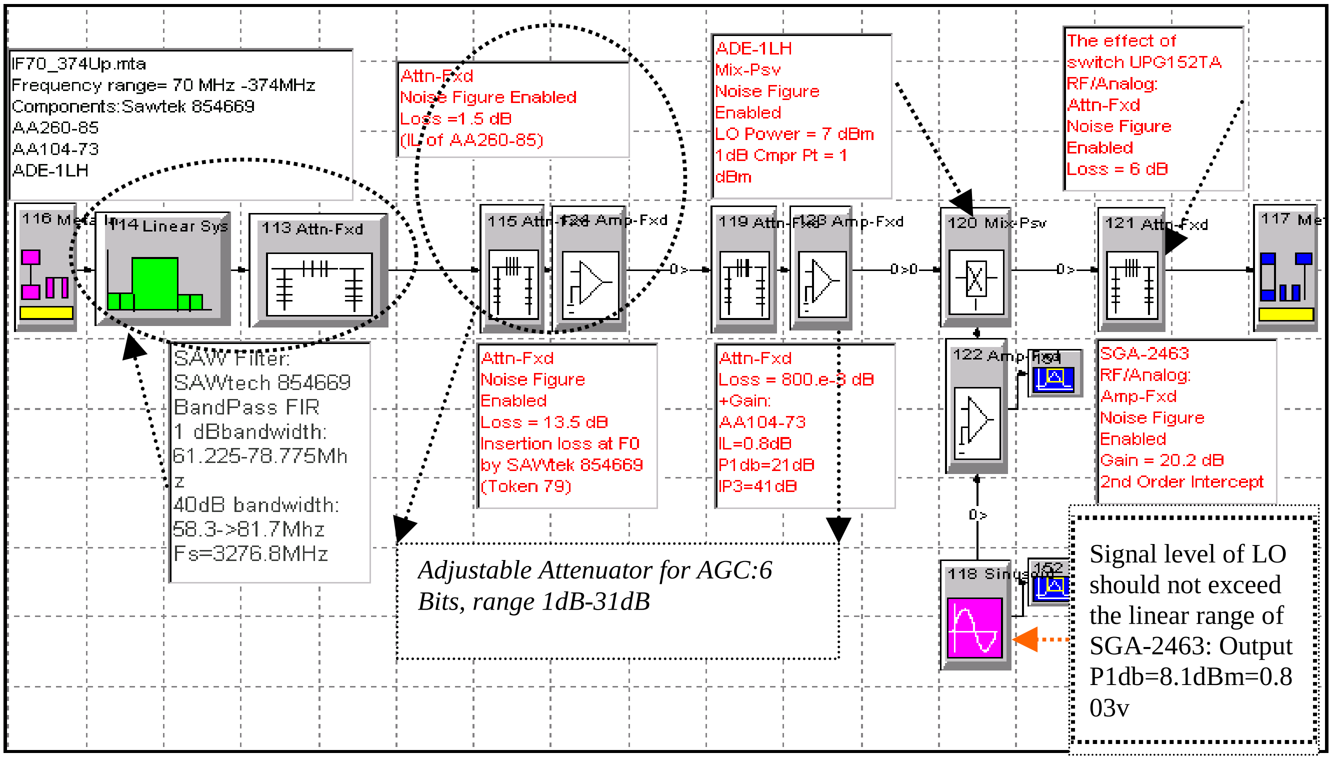
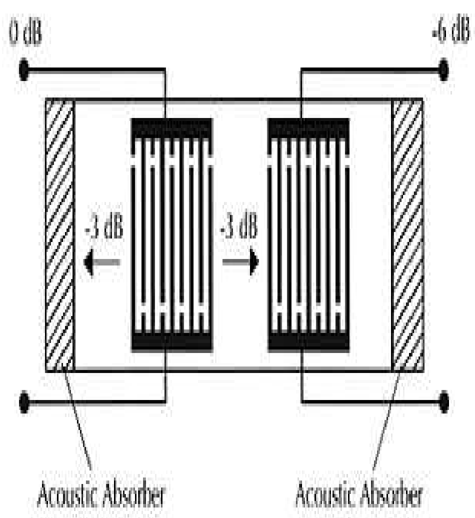


Fig. 4.11.1 Welkin IF system



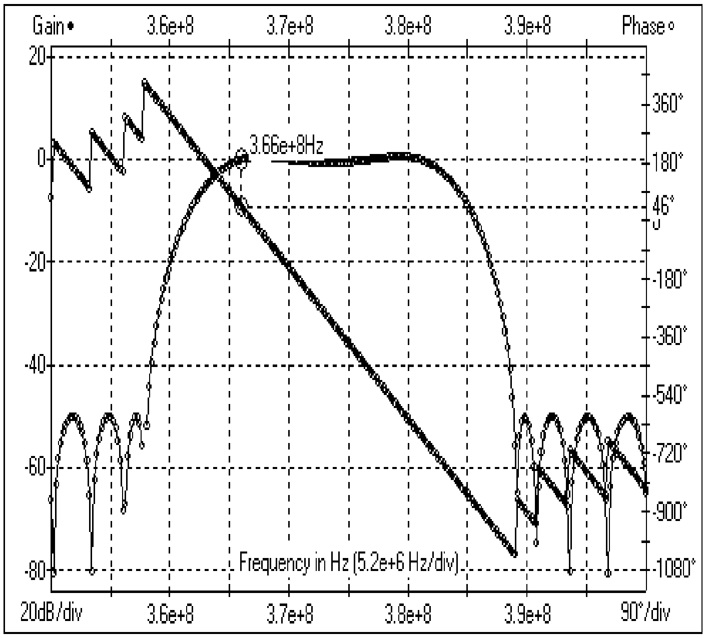


Fig. 4.12 SAW Filter *Fig.4.12.1 FIR to simulate the SAW Filter*

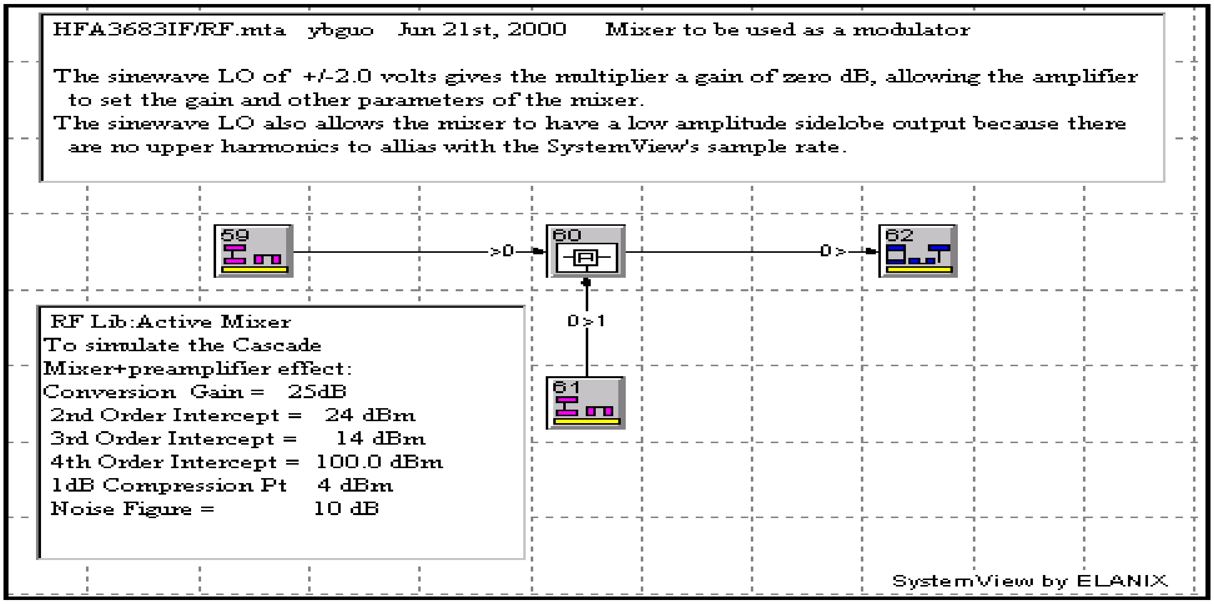


Fig.4.13 Active Mixer to simulate HFA 3683 IF/RF upconverter

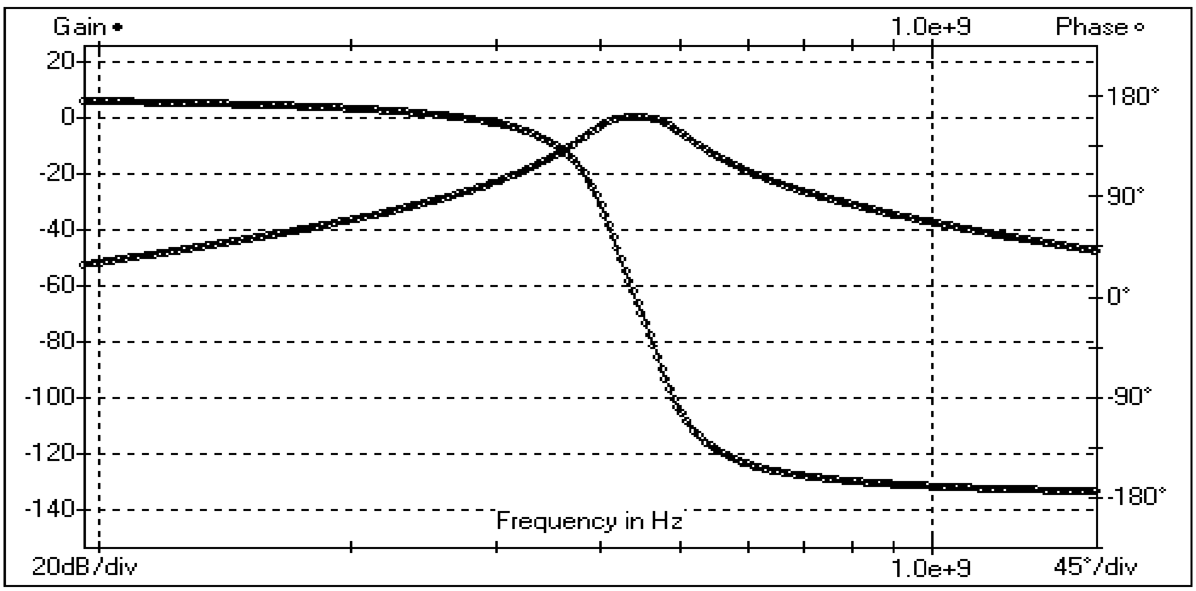


Fig.4.14 An analog filter used to simulate the prefilter DFC2442P084

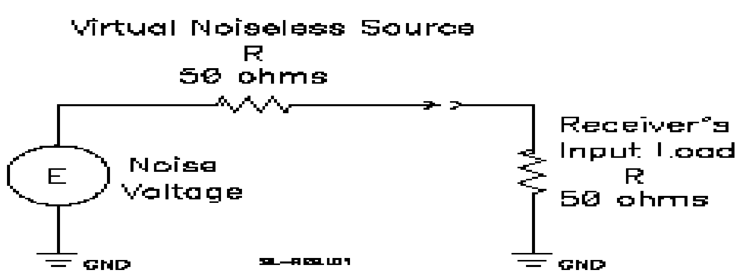


Fig.4.15 Circuit model of the receiver with thermal noise from antenna.

IF/RF upconverter

The design of IF/RF converter uses the Intersil HFA3683. Since now the frequency has been scaled, the local frequency is set to be 68 MHz and the RF is 442 MHz. Since the specification of HFA3683 only provides specification of cascaded mixer + power amplifier. The parameters are set as:

SSB Noise Figure	Output IP3	Output P1dB	Conversion Gain
10 dB	+14dB	4 dB	25 dB

Tab. 4.6 Cascaded specifications of mixer + power amplifier in HFA3683

To set these parameters, an active mixer is used instead of a passive filter and amplifier. The system is shown as in Fig.4.13. Since the PLL (phase lock loop) is integrated inside the RF/IF converter, it is not easy to simulate the effect from external. A careful analysis shows that for simplicity it is reasonable to just assume the input LO has a perfect frequency. A sine wave source is applied. Actually since the system rate is only 5 times of the RF frequency, the RF signal has some harmonics due to the effect of system sampling. In analysis, this should be taken care of.

Power Amplifier

The indicated HFA0589 can't be found from the Intersil web-site. So a typical power amplifier HFA3925 in the Prism chip-set is used here. Before the RF goes to the power amplifier, it passes through a DFC3-2442P084 bandpass filter. Since this filter is a dielectric filter, it is set to center frequency at 442 MHz with bandwidth with analog filter design. The specifications of the filter is:

Fo	Bandwidth	Insertion Loss	Ripple	30 dB Attenuation
442MHz(2,442 Orig)	84 MHz	2.4dB Max	1.0 dB	250 MHz

Tab.4.7 Specifications of DFC3442-84P filter

The phase and frequency response is shown in Fig.4.14. It almost matches the figure in DFC32 44284P perfectly.

4.4.3. Channel

The channel is combination of path loss to simulate the propagation and a thermal noise token to simulate the noise from receiver antenna. Notice that in the loss token the noise figure is disabled. The circuit model of the receiver is shown in Fig.4.15. In this model, the current in the receiver's input circuit is $I = E/2R$, where E is the noise voltage of the noiseless source resistor. Therefore, the input noise power is:

$$P_{noise} = I^2 R = \frac{E^2}{4R}. \tag{11}$$

Since the thermal noise due to a resistor is given by $V^2 = 4kTBR$,

Where,

K=Boltzman's constant, $1.38\times10^{-23} J/\deg K$,

T=Temperature, deg K,

R=Resistance, ohms,

B=Bandwidth,Hz.

So we get P_{noise}=KTB watts.

For a radio wave propagating in free space, the power falls off as the square of range. This effect is due to the spreading of the radio waves as they propagate and can be calculated by:

$$L = 20\log_{10}(4\pi D/\lambda) \qquad (12)$$

Where,

D = the distance between receiver and transmitter;

λ = free space wavelength = c/f and c is the speed of light 3e+8 m/s;

However for a different environment, the path loss relates to different model distance of range.

4.4.4. RF Receiver

LNA amplifier+RF/IF downconverter

After the signal comes from the antenna, the signal goes to the HFA3683A directly. An inherent image rejection allows the converter economic advantage. Similar to the transmitter, only specification of cascaded LNA amplifier and mixer is given. So here we still use an active mixer, this time with the following parameters:

Noise Figure	Input IP3	Input P1dB	Conversion Gain
3.7 dB	-13dBm	-23 dBm	25 dB

Tab. 4.8 Cascaded specifications for LNA + downconverter for HFA3683A

Actually the HFA3683A has a choice of high gain mode and low gain mode. In this simulation, we use the high gain mode.

The other parts of the system are self-explainary, except that different parameters are used according the different requirement of the architecture. The IF section of receiver is shown in Fig. 4.16.1. The mapping of the known parameter to the SystemView token is straightforward. However, in setting the simulation parameters, some components don't provide all the required parameters in a SystemView token. So we have to calculate the missed parameters based on the understanding of the physical concept of these parameters.

From the definition of P1dB, IP3,

we have that the following rules of thumb:

*Out P1dB = In P1dB * Gain(linear)-1dB= In P1dB+Gain(dB)-1dB;*

*Out IP3= In IP3 *Gain(linear)=In IP3 + Gain(dB);*

OutIP2=OutIP3+10dB;

OutIP3=OutP1dB+10dB;

InP1dB=InIP3-10dB+1dB;

The out IP4 of a component is usually not of interest, so it may be set to a high value (100dBm) to reduce its influence on the simulation.

Different components conventionally have a different reference of parameters. Typically, the mixer parameters are referenced to the input of the device. Changing the gain parameter of a mixer token will cause the clipping and saturation levels of the device to change also. For amplifiers, the parameters are referenced to the output of the device, so they directly indicate the clipping and saturation levels regardless of the amplifier's gain.

In selecting the different tokens from the library, we need to know the physical concepts of the parameters and the function of different token. For example, there is passive double-balanced mixer in contract to active mixer. Conversion loss, RF isolation, LO isolation and 3rd order harmonic are parameters to set. The details can be referred to the User's Manual and a textbook on RF circuit.

One key of RF design and modeling is to know how to analyze the signal waveform after adding a component. From the equation of cascaded noise figure, it can be seen that the first stage plays a more important role to the overall noise figure than following stages. So a low noise amplifier (LNA) with a low noise figure is used here.

The spectrum of each stage in the receiver is overlaid in Fig.4.16. The process of the change of spectrum in each can be analyzed in details. The signal has truly be modulated to 442MHz and then demodulated cascadely in each stage of the receiver. This analysis is critical in adding components or saving design cost. For the sake of limited volume of this report, the details will be omitted here.

Undersampling +ADC

The output of welkin IF has a 70 MHz frequency. To do IF sampling, a high-speed ADC (Analog Digital Converter) is always applied. Due to the sampling theorem, the sampling rate should be at least twice higher than the data rate to avoid a spectrum alias. However, ADC with such a high frequency is very hard to implement. If we review the sampling theorem of band-limited signal, we can design the sampling rate only at twice the data bandwidth. By using a sampling rate of 40 MHz and the effect of aliasing, the 70 MHz IF spectrum is shifted to center frequency of 10 MHz. A 12-bit quantizer again is applied to simulate the effect of ADC word length. This process is shown in Fig.4.17. while the mathematically formulation and diagram is as follows(omitted by far??).

Signal Level Analysis of Each Stage

Since the receiver has to detect very weak signal as low as –100dBm, it must obtain a very high gain. This gain is hard to achieve by one stage. This is one reason of the superheterodyne architecture. With the use of several RF components (amplifiers, attenuators and mixers), the signal level should be designed carefully according to the effect of non-linearity of each component. This is related closely to the selection of component parameters. For example, if one amplifier has a very high gain so that make the output signal level exceed the input P1dB compression of the next stage component such as mixer or attenuator, saturation will occur. Meantime, the input signal at the receiver can be in a wide range due to the distance of the transmitter to the receiver. This will demand the receiver have a wide dynamic range. This goal is achieved by the AGC (automatic gain control) at the attenuators in IF section. The input signal at the ADC should also be inside the range. With this knowledge, an analysis of the signal level in each stage is carried out.

A very important point is the interface of the IF to the ADC. The recommended ADC chip CLC 5987 has an input range of Vp-p=2.048 V. It is equal to 10.20 dBm and is larger than the output **P1dB** of SGA-2463, which is 8.1 dBm. In this simulation, the max input of the quantizer is set to $\pm 1\text{V}$. Some experiments also show that the ADC can work in a safe mode even when the SGA-2463 gets saturated.

The LNA constraints the maximum input level by its input P1dB, which is –23dBm. Also study the signal input at passive mixer ADE1LH. It indicates an input P1dB=5 dBm. If the input at this point is 5 dBm, the signal level at HFA3683 is –30.9 dBm since the signal from HFA3683 (+25dB) passes through the 374MHz SAW filter (-8.5dB), IF switch (-0.8dB) and the SGA amplifier (+20.2dB) before ADE-1LH. This is less than –23dBm, the input P1dBm of HFA3683, which means the LNA+downconverter will work in linear range but the passive mixer is saturated. So the ADE-1LH impacts the dynamic range of input more than the previous components. However, the SGA in this stage will always work in linear range with P1dB=8.1dBm. Another SGA is used to amplify the local frequency. With 20.2 dB gain and 8.1 dBm output P1dB compression, to make it work linearly, so the signal level should be less than 0.8V. Here 0.5V local frequency is used and generates about 3 dB at the mixed signal.

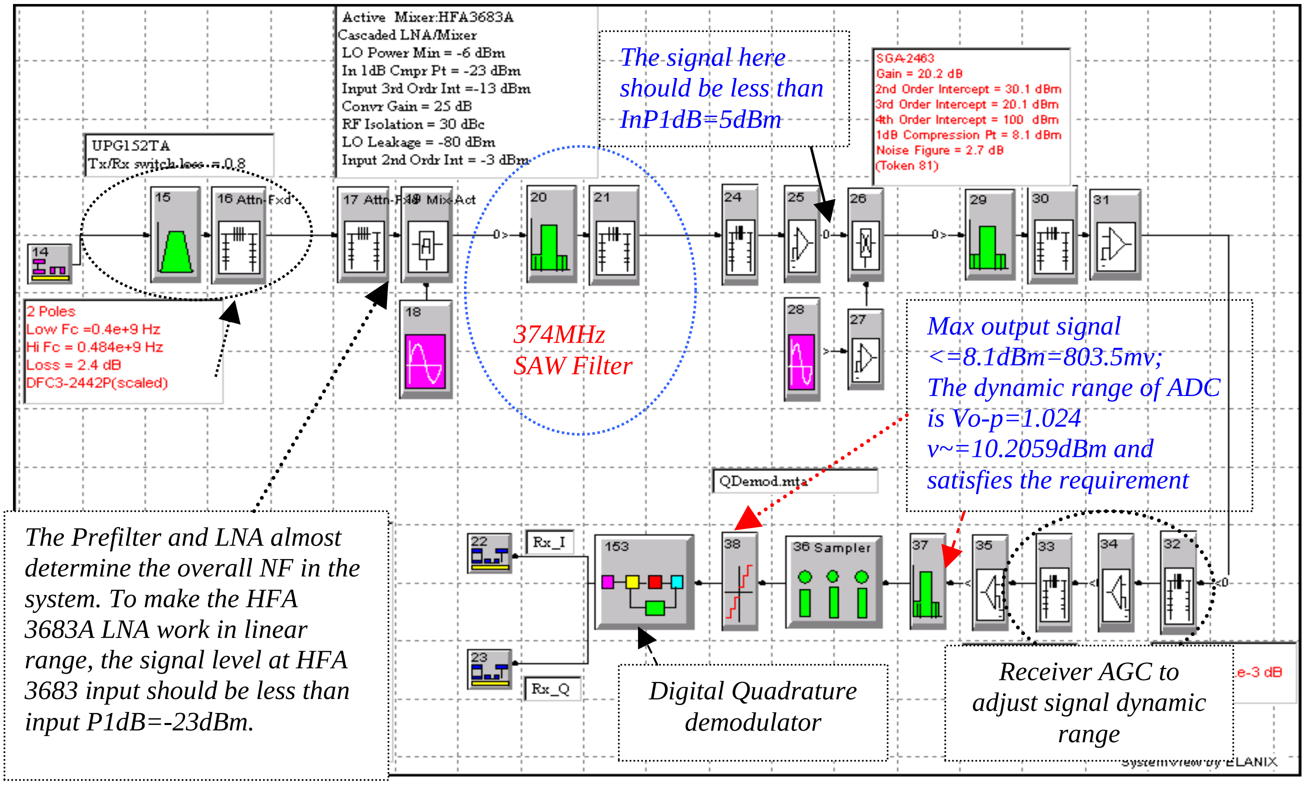


Fig.4.16.1. Welkin RF receiver. This figure includes the prefilter, HFA3683A RF/IF down converter, SAWFilter and IF section. The effect ofIF sampling ADC is also simulated here with a quantizer and sampler.

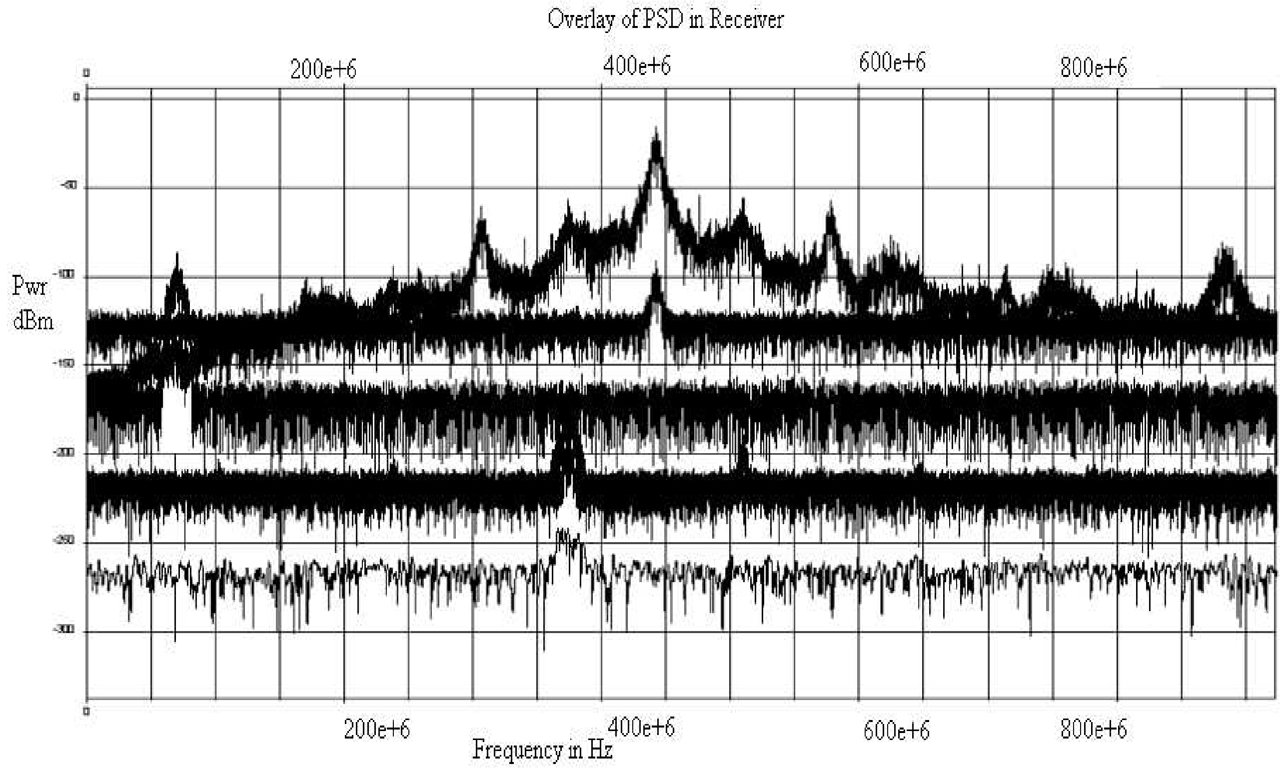


Fig.4.16.2 Overlay of the spectrum in each stage of receiver. For a clearer view, the plots are waterfalled with 30 shift in y axis.

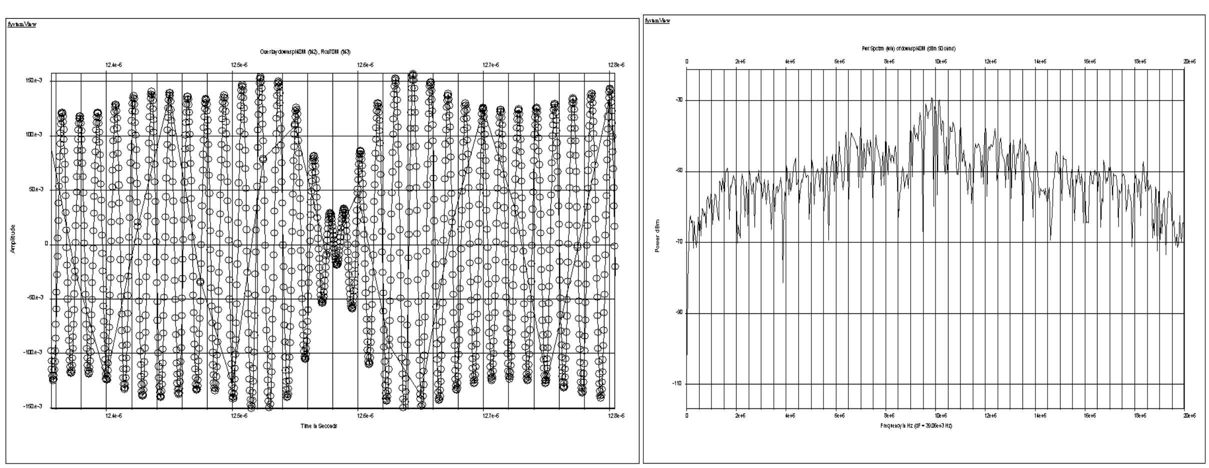


Fig.4.17. Downsampling with 40 MHz to achieve down-conversion. The spectrum is shifted to 10 MHz center frequency now.

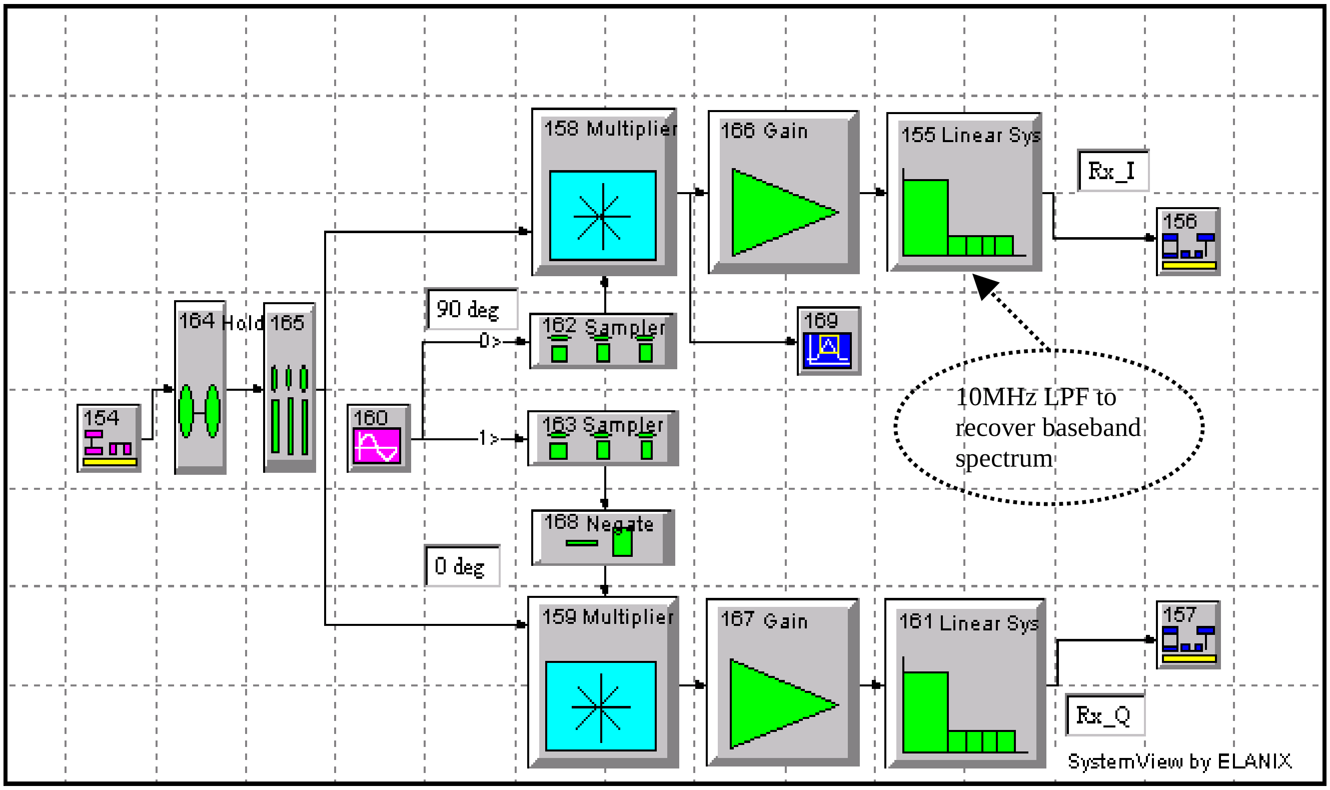


Fig. 4.18 The digital quadrature demodulator

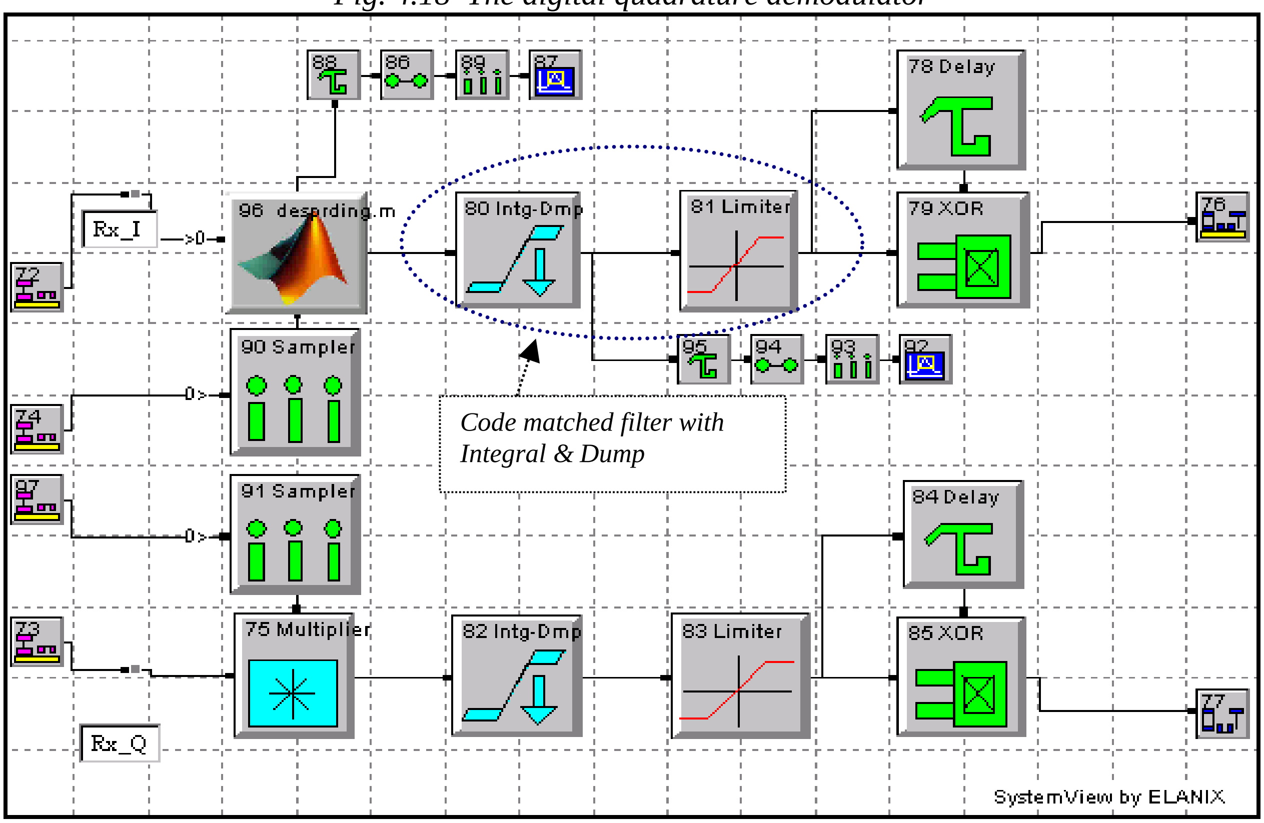


Fig.4.19. Baseband receiver. Code matched filter is implemented here with integral/dump and decision operation.

The two attenuators have input P1dB at 27dBm and 21 dBm respectively. This means that the signal at these two points will always be lower than this level and they work well. But notice that three SGA amplifiers are used at the 70MHz IF chain. Assuming the signal at ADE-1LH is 1dBm, the SAW filter has 13.6 dB loss, if the AGC attenuators has the minimum loss, then 5-3-5-13.6+20.2-0.8+20.2-1.5+20.2= 21.5dBm will exceed the linear range of SGA-2463 at the last stage. So the AGC must be applied at this point.
Summarily, the ADE-1LH passive mixer and the AGC attenuators constraint the maximum input signal level. If the signal exceeds this level with a short distance between the transmitter and receiver, the transmitter should turn down the transmitted power.

4.4.5. Baseband Receiver

Digital Quadrature demodulator

Now it is natural that a digital quadrature demodulator should be applied to recover the I/Q channel signal. 10 MHz LO is used here. This digital quadrature demodulator has the same advantage of direct digital synthesizer while implemented in DSP. A low-pass FIR filter with 10MHz bandwidth is used to derive the baseband spectrum (Fig.4.18). At this point, the complex signal is separated into two I/Q channel signals and recovered as the baseband signal. One thing should be pointed out that currently for simplicity, the carrier frequency is fixed to 10MHz. This is suitable only for a simple channel model with no frequency shift. In practice, carrier frequency recovery should be included for the phase error introduced.

Matched Filter Detector

To detect the received signal, a despreading process is applied. It has been known that the matched- filter is an optimal detector for AWGN channel, so a code-matched filter combining Integral/Dump token and a limiter is applied. To do the despreading, the spreading code should be synchronized with the received signal since there is a group delay in the transmission chain. The integral time has been set to be the length of one symbol bit: 1.0 ms. The limiter makes a decision that when the integral is greater than 0, a 1 is received, otherwise, a –1 is received. (Fig.4.19.)

Reconstructed Signal

To verify that the system works correctly and also for aligning the synchronization of the transmitted data bit and received data bit, Fig.4.20.shows the overlapped plots of the received signal after the code-matched filter, for both the baseband +AWGN and the RF scheme. For a clear comparison, the received the signal for baseband transmission is amplified by a gain of ***75 dB*** *(a regular gain without RF effects)*. This gain will not change the SNR of the received signal. The path loss used in this experiment is ***95dB*** and the transmitted signals of both schemes have the same amplitude level after the path loss: ***40e-6***. The thermal noise token used to simulate the antenna noise is set to a temperature of ***300K***. In this experiment, a length 7 gold code is used as the spreading code and repeated for each symbol. In this overlaid plot, the upper pair are the case of baseband signals while the lower pair are of the scheme with a RF transceiver. The flat lines are the result after the integral and dump token used as a code matched filter here. From the plot, we can see that the signal is reconstructed well. While it can also be seen somewhere that the baseband scheme has a flatter result from bit to bit, and the noise in the rectangle pattern envelop is more averaged as white noise than the scheme with RF section. This implies that the RF transceiver introduces some distortion to the system and may generate higher bit error rate. We can see that for this limited section, the recovered bits match the input bits perfectly with zero errors. This means the BER measurement subsystem works well and the measured BER is accurate.

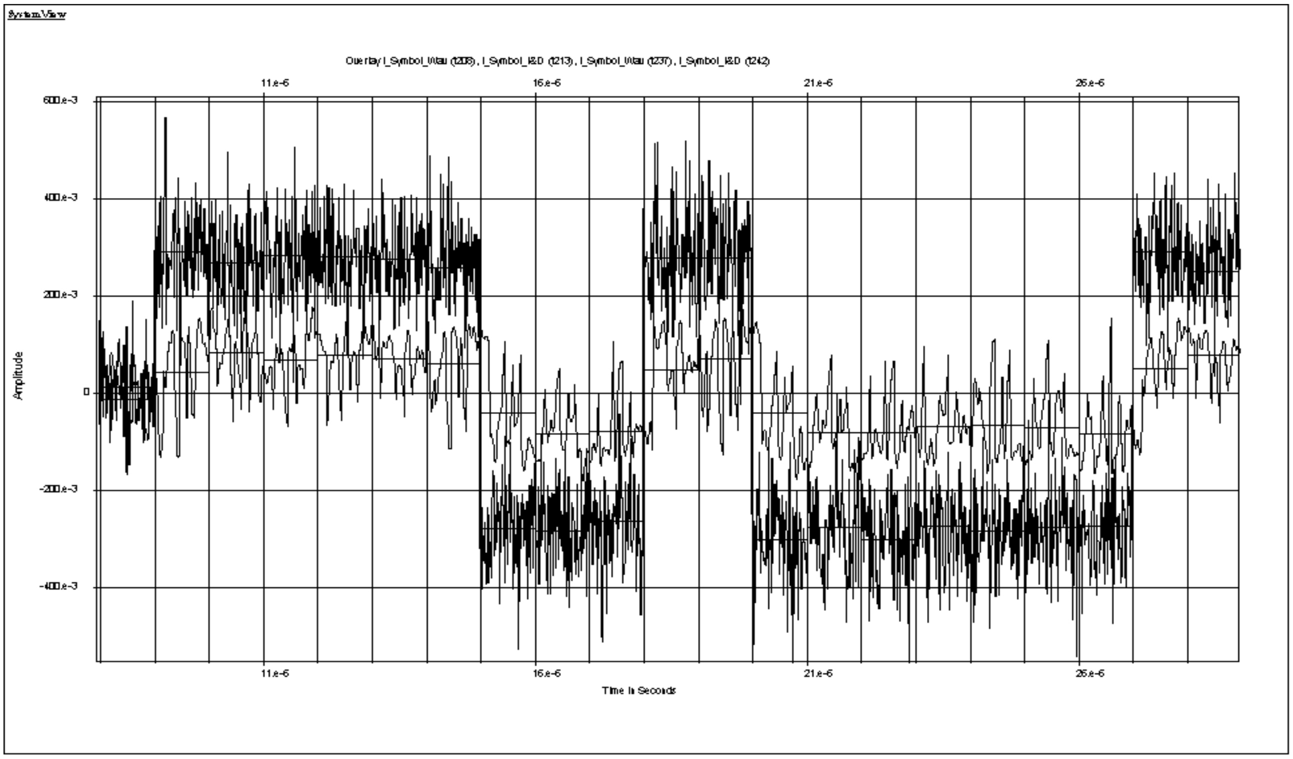


Fig.4.20.1 The overlay of receiver signal for a system with RF and without RF

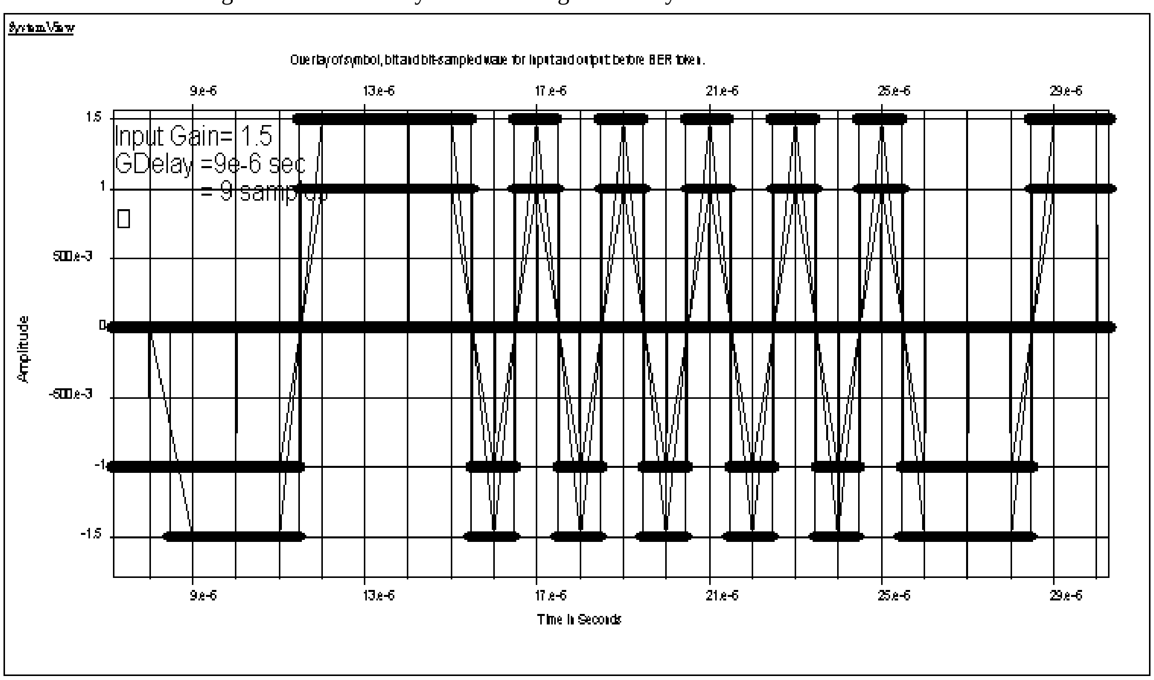


Fig.4.20.2 Overlay of the input data and output data

4.5 BER Measurement Subsystem

Fig 4.21.1 shows the subsystem to detect the **BER (bit error rate)**, which is calculated as the rate of errors over the overall transmitted bits. The inputs to the BER token are 1 sample per bit from both the input and the recovered bit stream. Since there is a group delay on the processing, the start time of BER measurement should be set after the delay and the input and output should be synchronized. To get a correct sampling, the sampling point should be chosen to be in the middle of the pulse. The BER token has several parameters. It can be set to calculate frame error rate **(FER), BER, SER(symbol error rate)** while setting the number of trials to different number. A cumulative token $y(t) = G.\frac{1}{T}\int_0^t x(\alpha)d\alpha$ is used to calculate the running BER. To save memory, a final value sink is used to discard the intermediate values.

The number of bits to run in a simulation is determined on the BER level required. One way to generate the BER curve is to set a large number of trials in the time window, large enough to accommodate the number of trials required for the lowest desired BER. However, a careful review will unveil that this is an overskill. As long as the simulation is long enough to accumulate a stable BER the simulation can be stopped. The number of trials varies in this case. To optimize the simulation time, a simple counter using a digital filter $H(z) = 1/(1 - z^{-1})$ and stop sink token are applied. As the error meets the number defined in the stop sink, say, 100, the simulation for this loop stops and continues to another loop. To control the SNR per loop, the path loss is set to be a global parameter and connected to the loop number. Thus, by setting the loop number, a BER curve can be generated automatically.

Fig.4.21.2 shows the BER vs. time for several loops. The jump means another loop with a less path loss. From the shape, it is clear that the BER is stable after some time. The time for BER to converge increases as the path loss decreases. The result of BER curve is analyzed in the next section with the effect of RF to the receiver sensitivity

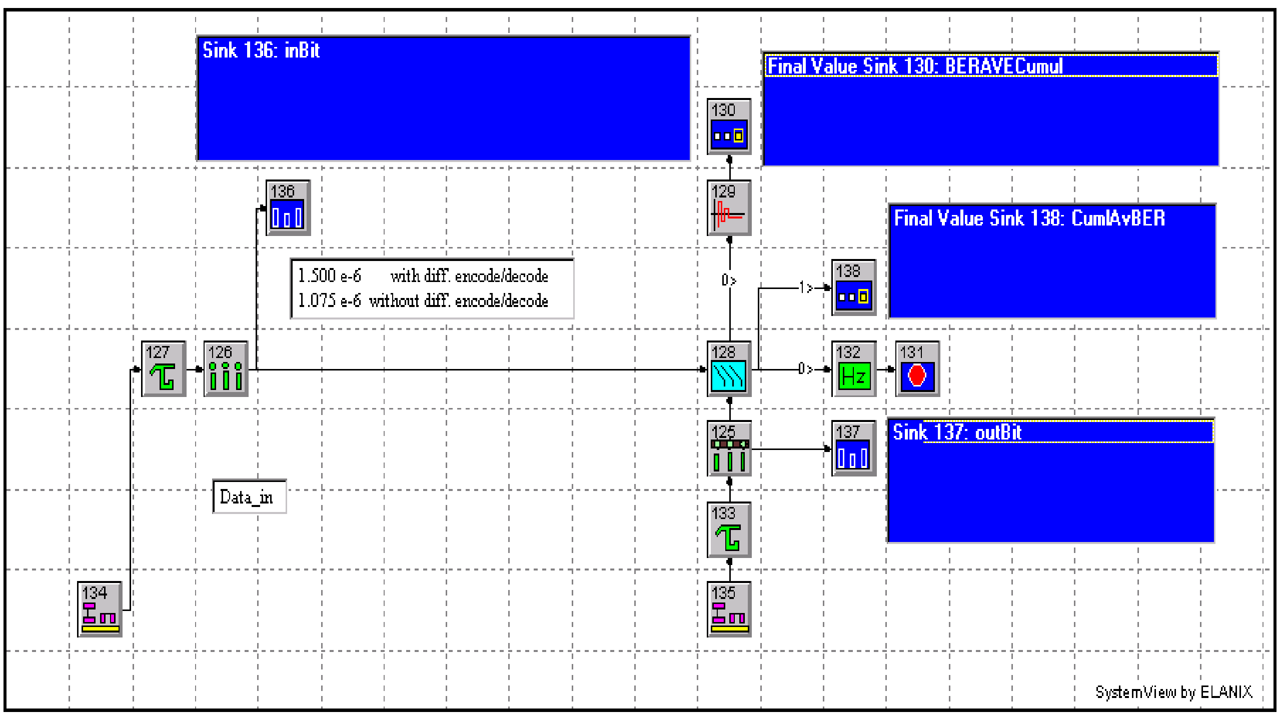


Fig.4.21.1 Subsystem to detect the BER result

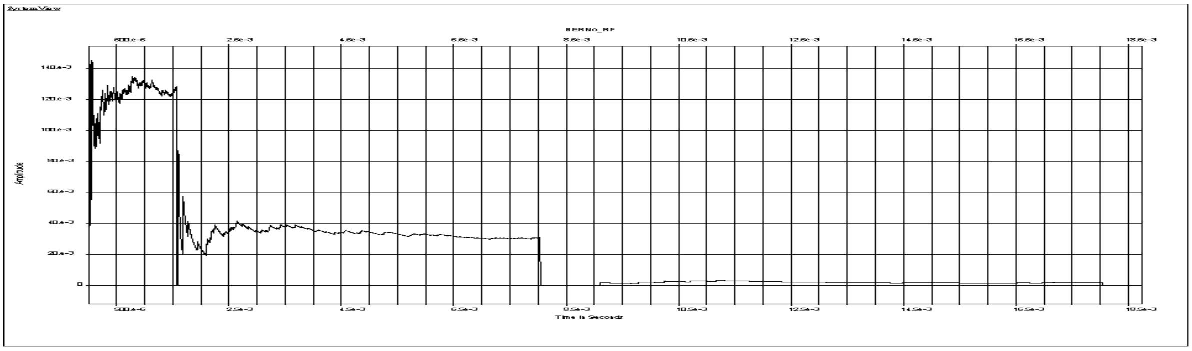
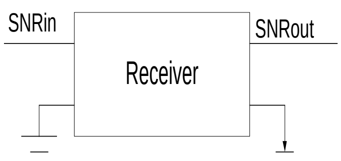


Fig.4.21.2 BER vs. time shows that the time for convergence increases as the BER becomes smaller.

4.6 Receiver Sensitivity

Depending on a particular digital communication application, the digital communication system requirements impose different RF transceiver specifications for the same parameter value. One of the fundamental system parameters often faced by RF transceivers at the beginning of a design is *bit energy requirement* of the system.

To achieve a particular BER requirement, the sensitivity of a receiver is of interest. The sensitivity of a RF receiver is defined as the minimum signal level that the system can detect with an acceptable SNR. For simplicity, the receiver can be modeled by the following figure with SNR_{in} *at input and* SNR_{out} at output.



From the definition of noise figure, we have,

$$NF = {SNR_{in}} \Big/ {SNR_{out}}$$

$$= \frac{P_{sig} / P_{Rs}}{SNR_{out}} \qquad (13)$$

where the Psig is the power of signal and P_{Rs} the power of noise caused by the thermal noise at the input of receiver. To calculate the minimum level of the input signal, we have,

$$\Rightarrow P_{sig} = NF \bullet P_{Rs} \bullet SNR_{out}$$
$$\Rightarrow P_{sigtol} = NF \bullet P_{Rs} \bullet SNR_{out} \bullet B \qquad (14)$$
$$\Rightarrow P_{sig\min}\,|_{dBm} = P_{Rs}\,|_{dBm/Hz} + NF\,|_{dB} + SNR_{out\min}\,|_{dB} + 10\log B$$

By assuming conjugating matching at the input, we obtain P_{Rs} as the noise power that *Rs* delivers to the receiver, where *Rs* is the input resistance of the receiver. By including the implementation loss, we get,

$$Estimated\,\mathrm{Re}ceiver\,Sensitivity = kT + NF\,|_{dB} + 10\log B\,|_{dB} + SNR_{out} + \mathrm{Im}\_Loss \qquad (15)$$

By defining,

$$RcvrNoiseFloor = kT + 10\log(B|_{Hz})|_{dB} + NF(dB) \tag{16}$$

we can write,

$$Est\_Rcvr\_Sens = Rcvr\ Noise\ Floor + SNR_{out} + \mathrm{Im}\_Loss \tag{17}$$

Assuming T=300 deg(room temperature), we have P_{Rs} =*kT=-174dBm/Hz* from (11). If we know the noise figure of the system, then we can calculate the receiver sensitivity.

However the direct calculation of NF is difficult. One way is to handle this problem inversely by generating the BER curve and reading the corresponding sensitivity directly from the curve and then calculate the NF. Another way is to compare with a baseband scheme. To get the required SNR for one modulation, a reference system with only baseband scheme is used as a benchmark. The theoretical results of non-coherent DPSK, coherent DPSK and coherent PSK are also used here in Fig.4.22. The simulated baseband result matches the theoretical non-coherent DPSK almost perfectly, indicating that the simulation result is correct (Fig.4.22).

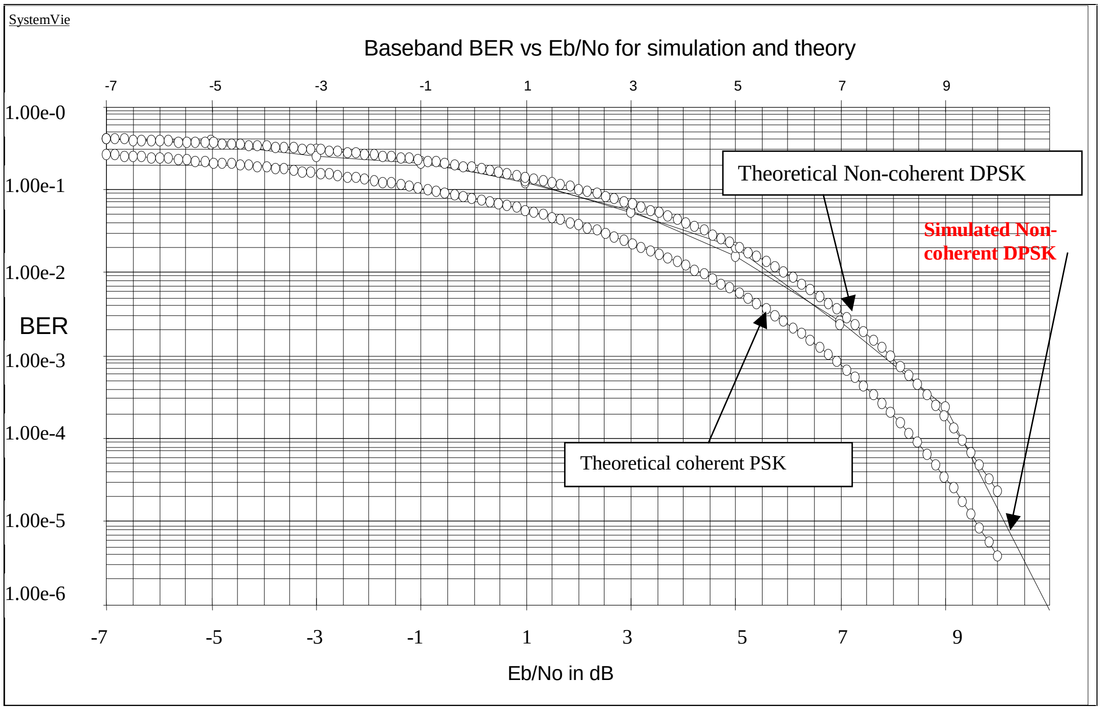


Fig 4.22 BER vs SNR for a system without RF and the theoretical result for DPSK, ODPSK, BPSK

From (11), $P_{noise} = kTB$, so the SNR of the baseband scheme can be calculated by

$$SNR_{BB} = \frac{P_{RXBB}}{P_{noise}} = \frac{P_{TXBB}/Loss_{BB}}{kTB_{BB}} = P_{TXBB}|_{dBm} - Loss_{BB}|_{dB} - kT|_{dBm} - 10\log(B_{BB})|_{dB} \tag{18}$$

So, if the scheme with RF has the same BER with the baseband scheme for a same modulation, the Required SNR should be the same as the baseband SNR. Since

$$
\begin{cases}
SNR_{BB} = P_{TXBB} - Loss_{BB} - kT - 10\log(B_{BB}) \\
SNR_{out} = P_{TXRF} - Loss_{RF} - kT - 10\log(B_{RF}) - NF \\
SNR_{BB} = SNR_{out}
\end{cases}
\tag{19}
$$

then,

$$
NF = (P_{TXRF} - P_{TXBB}) + (Loss_{BB} - Loss_{RF}) + (10\log(B_{BB}) - 10\log(B_{RF})) \tag{20}
$$

Fig.4.23 shows the overlay of *BER vs. path loss* for baseband scheme, a W-CDMA with Gold-7 code. In this simulation, the baseband TX signal has the same level as the RF scheme. At BER of *2.4e-3*,the RF chain introduces a loss of 14dB over the baseband scheme. The base band bandwidth is 7MHz while the RF bandwidth is 14MHz. So the NF can be calculated as 14.5 dB- 3 dB = 11.5 dB. Since the transmitted output signals have 5v amplitude. The receiver sensitivity of BER about 1.5e-3 reads about 23.98-119 = -95.02 dBm.

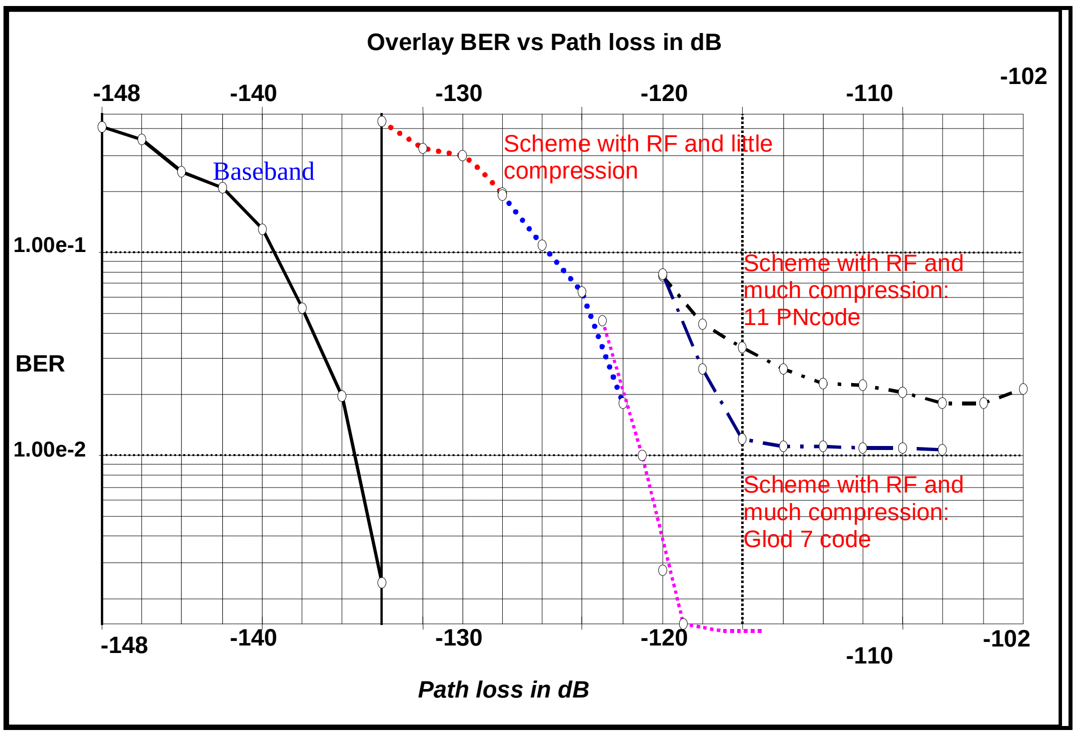


Fig.4.23 BER vs. Path Loss for reference system without RF and the system with welkin RF section

The effect of saturation is also studied. The right two curves are the result when the quantizer is saturated at the transmitter and also the attenuators in transmitter chain only used the minimum attenuation, so that some non-linearity appears. Both the two curves become flat at some point. This means that the system was not adjusted properly and got saturated. The effect of different spreading gain is also compared with the use of 11MCPS and 7MCPS chip rates. It is clear that a higher chip-rate, decreases the BER performance.

The welkin RF system design goal specifies a NF =10dB (theoretical +implementation loss) at Pin=-97dBm and a receiver sensitivity at about –97dBm with 500kHz chip rate. It does not indicate the BER requirement at this point. From the equation of Receiver sensitivity,

$$\begin{aligned} SNR &= 174 + S_{rcv} - 10\log(2\times B_{chip}) - NF \\ &= 174 - 97 + 10\log(10^6) - 10 \\ &= 7(dB) \end{aligned} \tag{21}$$

So we estimate that the sensitivity of BER is at the order of 1e-3.
From the analysis, the simulation result is close to the design goal. There is some margin at the theoretical calculation and the simulation result. This may be caused by various reasons. The quantization noise, the synchronization of receiver both for frequency and spreading code and the simulation itself can all introduce some noises. Even though, this simulation can be used to verify the design and test the signal features in each stage of the transceiver. It provides an analysis method by including the non-linearity effects of real components. It can also used to study the effect of RF on other more complicated modulation schemes.

Compared with the Welkin system design goal which indicates a NF=10 dB with Pin = –97dBm and a NF=36dB at Pin=-20dBm, this analysis is again reasonable. This means the noise figure will increase as the input signal level increases dramatically. We can see that a Pin=-20dBm even exceeds the input P1dB compression of the first stage LNA, which is –23dBm. A coarse calculation of the gain in the receiver chain shows that this will cause a large saturation at the receiver end. The simulation verified this by studying the signal waveform at high input. The waveform became flat top then. This tells us that power control is critical to the receiver's sensitivity. This introduces one question, how to control the transmission power and keep a level of quality of service (Qos) requirement (here the BER requirement) while the path loss changes? It will be very hard to calculate the reference values directly. But maybe we can carry out a scenario of simulation which makes the path loss change and changes the transmission power to see if it is possible to keep the BER constant.
Tab. 4.9 summarized the comparison of the simulation result and design goal.

	Welkin Design Goal	**Simulation Result**
Receiver Sensitivity	-97dBm at 500KHz chip rate(BER=?? Guess 1.0e-3 with SNR=7dB)	-95.02 dBm at 7MHz chip rate (order of 1.00e-3 BER and SNR=8dB)
Noise Figure	(1) 10dB: Theoretical+Implementation loss at Pin=-97dB (2) 36dB at Pin=-20dB	(1). 11.5dBm at Pin=-95.02dBm and chip rate 7MHz (2). Increase as Pin increases

Tab.4.9. Comparison of the simulation result with Welkin design goal

One important thing should be pointed here. The equation of cascaded noise figure indicates that the noise contributed by each stage decreases as the gain preceding the stage increases, implying that the first stages in a cascade are the most critical. Conversely, if a stage exhibits attentuation (loss), the NF of the following circuit is "amplified" when referred to the input of that stage. This occurs for example, if a narrowband lossy filter is interposed between the antenna and the low noise amplifier in a receiver to reject out of band interference.

So the overall noise figure of a lossy filter followed by a low-noise amplifier,

$$\begin{aligned} NF_{tot} &= NF_{filter} + \frac{NF_{LNA} - 1}{L^{-1}} \\ &= L + (NF_{LNA} - 1)L \\ &= L \times NF_{LNA} \end{aligned} \tag{22}$$

Another important factor is the noise figure of lossy circuits. In passive reciprocal network, the noise figure is equal to the loss if the latter is defined as,

$$NF = 4KTR_{out} \cdot \frac{V_{in}^2}{V_{TH}^2} \cdot \frac{1}{4KTR_s} = L \tag{23}$$

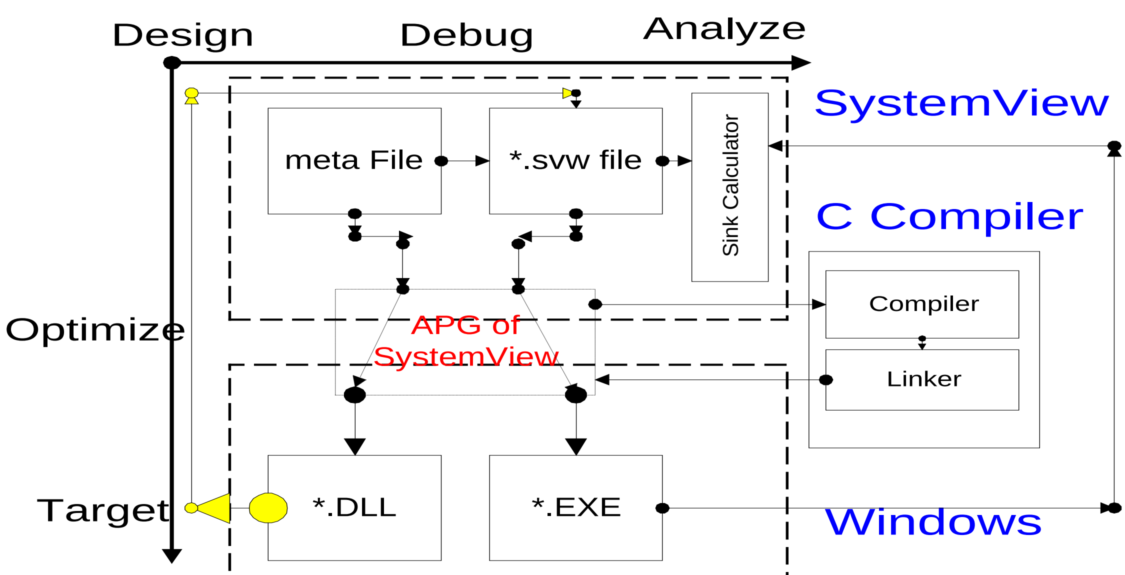
4.7. Optimization of the Productivity

As mentioned earlier, the analog simulation is actually done on a digital computer. With the high carrier frequency, the system sampling rate is always prohibitively high, which makes the run-time very long, especially when calculating BER curve. So one may demand some optimization methods for higher productivity.

Two methods have been mentioned as frequency re-planning and multi-rate operation. Special attention should be paid to the spectrum changes that may be introduced by these operations and a clear concept of sampling theory and a comprehensive knowledge of the available samplers is demanded while choosing from several different tokens with different functions in the library.

Generally speaking, down-sampling can be achieved by re-sampler and decimator. Interpolate or non-interpolate modes can be selected and these options are self-explainary. While in upsampling we need more attention, since the new samples can be held as the last sample, which means it is a flat-top sampling, or can be interpolated. The judgement depends on the analysis of the real signal waveform in the link.

Another special feature for optimization supported by SystemView is the ***APG (Automatic Program Generator)*** option. APG is a tool to create 32-bit windows executable programs from SystemView complete system Designs or ***DLL* (Dynamic Link Library)** from SystemView meta system. The main purpose of this option is to make the program much faster.
The design procedure with **APG** is summarized as the following diagram:



Design Flow with APG in SystemView

In the development plane, we divide the process into two domains. One is the process of *design* ->*optimize* -> *target* programs. The other axis is the domain of *design*->*debug*->*analyze*. The system is first defined as several meta systems. Each meta systems is debugged and the results analyzed. As the subsystem is fixed, it can be generated to a *.dll costum token to improve the running time. Notice that to make a *.dll , the meta system can't include any sink tokens. As all the subsystem has been debugged, the complete system can be generated as independent Windows executable file, i.e., the target. (Currently the APG only supports windows executable file, but it is aiming to generate TI's C6000 executable files). The compiling and linking procedures are done by Microsoft C compiler. It is clear that the system works in several domains.

From this process, we can see that a clever partitioning of the models is very important, both for result analysis and model reuse. It should also be pointed out that in a SystemView simulation, the analysis process is as important as the design process. The analysis window includes a powerful sink calculator that provides tools for performing operations within, or between individual plot windows. So we need to study the commonality of different schemes to make it adjust to further change.

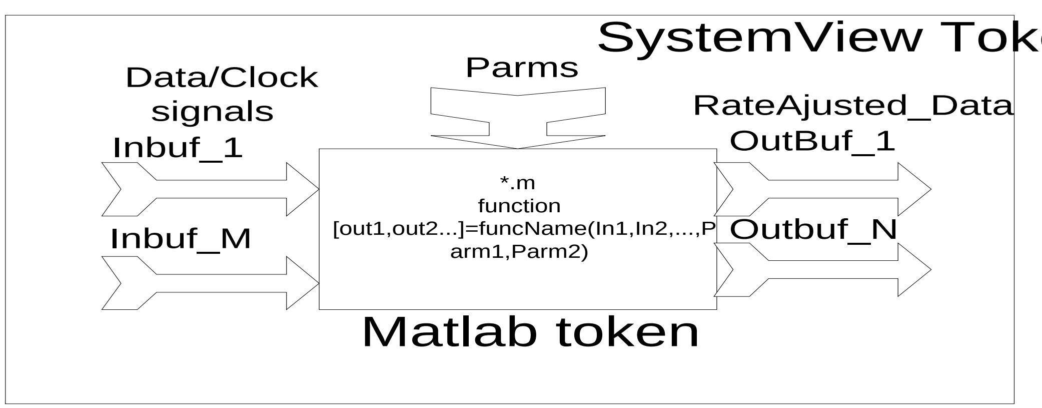
4.8 Extendable Architecture

Although the current system is designed to measure only the BER of I channel, so that the BER result is actually of non-coherent DBPSK, the system has the Q channel for extension to any quadrature modulation scheme. An easy way to change it into QPSK scheme is to change the baseband transmitter and receiver with two channel input/outputs, then add the bit-to-symbol mapping part as the feed in of I/Q channel.

Interface with Matlab

SystemView provides the interface with Matlab "*.m" files and Simulink "*.mex" files. This feature supports the use of third party Matlab lib and custom Matlab script easily, making it possible to reuse the previous work so as to improve productivity.

This figure shows the communication between the SystemView and Matlab functions. The inputs for a Matlab function can be mapped to the inputs and parameters of a Matlab token in SystemView. Typically, options used to control the Matlab function are mapped to parameters while data mapped to inputs. For both inputs and outputs, SystemView handle the buffers automatically. The length of the buffers can be defined by the user. The Matlab token can be defined as source, general or sink token depending on the number of inputs and outputs. However, one thing should be paid special attention to. In Matlab simulation, there is no system time. However in the simulation of SystemView, system time is set absolutely. So the input to the Matlab is also used as a clock signal. Each time the Matlab function is called, the input buffers are filled and the output buffers are emptied.



Communication of Matlab &SystemView

In our current system, the spreading and despreading tokens are designed as Matlab custom tokens. The spreading token takes the original data bit after the differential encoder as input, codeType is defined as a parameter. Then the token first generates a short code according to the codeType, then does spreading with the inBit. Both the spreaded chips and the spreading code are sent as output. When using MATLAB engine, since there is a communication between Matlab and SystemView, the running time increases dramatically. In our current simulation where 10,000 bits are used, 10 hours are needed to run 10 loops without matlab token, while 79 hours are needed for 8 loops with Matlab spreading/despreading tokens. This time may be reduced by increase the buffer length between Matlab and Systemview with a group processing.

5. HARDWARE DESIGN CONSIDERATIONS

5.1 Component Requirement

Small Desired Signals vs. Strong Interference

The design of the RF system depends much on the availability of related components. Practical issues such as cost, size, power can't be reflected in a software simulation, however they are very important factors in determining the selection of the components and design, even the architecture. Although in the software simulation of the RF system, only the main effects such as non-linearity are taken into consideration, special attentions should be paid to the selection of the parameters. Considering the building blocks, there are oscillators, mixers, amplifiers and filters. Because of the different function of these components in each stage, the requirements are different. For examples, in a sense of ideal component, LNA(low noise amplifier) and Power amplifier is as simple as just a gain. But in a practical sense, they are pretty different in the sense of gain and noise figure.

Receivers must be very sensitive to small input signals. Typically, receivers are expected to operate with as little as 1uV at the input. The sensitivity of a receiver is limited by the noise generated in the input circuitry of the receiver. The noise performance of the front end is determined mainly by the LNA, the mixer and LO. The small input signal level requires that receivers must be capable of a tremendous amount of amplification. Often as much as 120dB of gain is needed. With such high gain, any coupling from the output back to the input can cause problems. One important reason why this superheterodyne receiver architecture is used is to spread that gain over several frequencies to reduce the chance of coupling. It also results in the first LO's being at a different frequency than the input, which prevents this large signal from contaminating the small input signal. For various reasons, the direct conversion or homodyne architecture is a candidate to replace the superheterodyne architecture in some wireless communications systems. In this case, the ability to determine the impact of small amounts of coupling is quite important and will require careful modeling of the stray signal paths, such as coupling through the substrate, between package pins and bondwires, and through the supply lines. They make the problem double difficult.

The passive devices often determine the overall size, topology and the performance of a wireless communications transceiver. These elements include inductors, filters, resonators ,and capacitors. Many of these elements are difficult if not impossible to integrte monolithically.

The development of surface acoustic wave (SAW) devices is one of the most important developments in the field of wireless communications. These devices are typically bandpass filters with very sharp and stable cutoff characteristics. One drawback of SAW devices is their relatively high insertion loss, which creates the need for pre and postamplification around the circuit.

Reviewing the performance of the building blocks in an RF system, the special requirements of each component are summarized here.

- Duplexers with low insertion loss, usually, a duplexer adds an additional 3-dB noise figure in the receiver and 3-dB power loss in the transmit paths at 800MHz; Commercial duplexers available for cellular telephone industry use have the largest physical volume of all other RF components in the transceiver. In handheld portable equipment, the duplexer dimensions and its losses can be a real problem in the enclosure design and the battery life considerations.

- Low noise amplifiers(LNAs) with high intercept point and low current consumption; Perhaps one of the hardest specifications the designer of an RF transceiver faces is the balancing act between the receiver sensitivity and the intermodulation requirements in conjunction with full transmit power.
- Mixers with high intercept point and low noise; It is commonly recognized by experienced designers that the selection of the first mixer design topology dominates the receiver chain performance. The mixer perfornance consideration is accentuated by the need to provide good local oscillator(LO) leakage isolation while maintaining a good balance between the front-end noise figure(NF) and intermodulation isolation. One common design approach replaces the front-end LNA with an active low-noise first mixer.
- Filters with low thermal center frequency drift and frequency response tolerance;

A study of the parameters show that the components selected in the current design satisfy these requirements.

Digital Direct Synthesizer

There is a rapid migration afoot toward all-digital communications channels. The advantages of digital formats are obvious at direct processor control, on-the-fly programmability and configurability, precision frequency hopping and fine-tuning. These attributes have been enhanced with the breakthroughs in several high-speed components.

As well as single-tone local oscillators and clock generators, DDS solutions are also being integrated into digital modulator and upconverter architectures. Analog Devices has two innovative products that integrate the DDS. In the AD9865 quadrature digital upconverter device, the DDS is used to generate the sine and cosine carriers that are modulated with complex data from the 12-bit data port. This device eliminates the complexity and loop settling time issues associated with an analog-based upconverter stage. As they claim, the AD9856 represents a true breakthrough in IC communications technology. The advantages are summarized as:

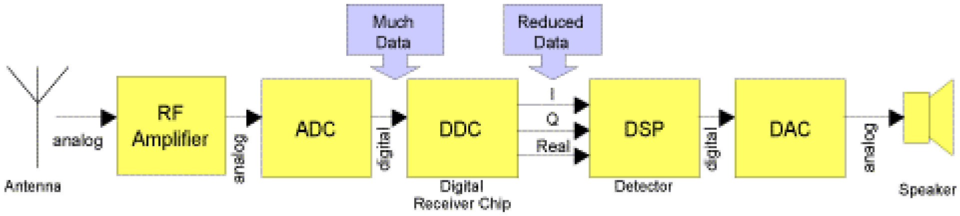
- By performing the modulation in the digital domain, the benefits of perfect I/Q channel matching, precise digital tuning and fast channel hopping can be utilized to the fullest extent;
- As seen from the simulation block, the AD9856 can perform a digital upconversion on any complex data stream (QPSK, QAM, spread-spectrum, MSK, GMSK, etc).
- The programmable interpolation filters support a wide range of data rates and applications at input sample rate of up to 50 MSPS.
- The AD9856 QDUC(Quadrature Digital Up Converter) device allows system partitioning to separate the digital signal processing circuitry from the mixed signal RF interface. Partitioning removes the risk and yield impact associated with attempting to integrate mixed-signal functions onto deep submicron CMOS digital ASICs. This concept of SSP (smart system partitioning by intentionally separating RF interface and digital ASICs) introduces optimal performance;
- By exploiting the high degree of flexibility in the AD9856's architecture, the system designer can maintain a more "future proof" system.

The recently delivered AD9857 builds on that legacy by delivering the world's best spur and noise performance for the integrated QDUC function and can be another choice.

As for the down-converter at the IF to baseband interface, the requirement for wide band and narrow band application is different. For a narrow band application, the I/Q signal can be separated in analog part and then sampled with ADCs. While in a wide band application, like in our design, the signal is first under-sampled at 40MHz. So the separation of I/Q is realized through digital techniques. Now several key technology breakthroughs are required: high dynamic range ADCs, new DSPs (highly programmable with onboard memory, fast), digital tuners and filters, wide band mixers and amplifiers. In the literature of high-speed design, special ADCs for IF sampling are a category. Even though, the high speed of digital down-conversion and filtering may be still too high for general purpose DSPs. There is some research on the FPGA implementation of digital receiver which includes digital frequency tuner and LPF. However, if we can find the corresponding counter part of the DDS/upconverter, it will save the computation cost of DSP.

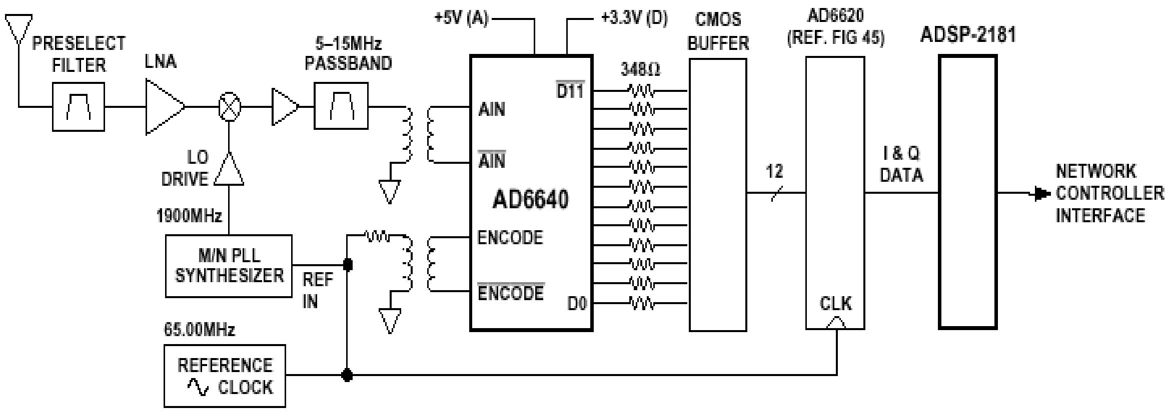
Digital Down Converter

As at the receiver IF and baseband interface. AD6640 may be a good choice for IF sampling and AD6620 can be combined to do the digital quadrature demodulator. In the design of high speed all digital receiver, one challenge is the high-speed ADC for IF sampling and digital quadrature demodulator. Even though the DSP technologies have developed fast, the speed of W-CDMA is still somewhat too high for general purpose DSPs. For wide-band applications, some research has been carried for a new family of components: DDC (Digital Down Converter).The idea is to apply another DDC component between the high-speed ADC and DSP, as the following figure shows.



Simplified Digital Receiver System

Although the DDC does the same function as the conventional counterpart, it has several new features and is always programmable. Because of the high-speed and wide-band requirement, it is still a very new market in industry. So a survey of the availability of such components is essential to our system. AD6620 is a new DDC (digital down converter) which integrates cosine/sine mixer and filters. The following figure shows a simplified PCS digital receiver with AD6640 and AD6620. The features of these components will be studied further.



A simplified wideband PCS digital receiver with AD6640+AD6620.

Summarily, although RF technologies have been developing for many years, it is still progressing with a lot of interesting new issues such the architecture and digital technique. The use of digital transmitter/receiver which shift the digital part closer to the RF front-end also reflects the popular idea of software radio by introducing more flexibility and programmability to the RF signal.

The literature survey of high-speed DAC/ADC (digital up/down converter) was divided into several levels: (1). to study the trend of RF/baseband design; (2). To study available chips supporting the specification; (3). To search if there is available modules for our DSP/RF interface. For limited volume, they are not included in this report.

6. CONCLUSION AND FUTURE WORKS

In this work, we built a complete W-CDMA system to model Welkin RF system. The simulation of RF system took parameters from real world components and considered the non-linearity effects of RF circuits. By analyzing the activity of the RF, we figured out the baseband interface and applied some simple schemes for the simulation, such as a DPSK, spectrum/spreading and code matched filter. To improve the spectrum efficiency, pulse shaping with raised cosine filter was applied. Various kinds of methods were used to analyze the RF effects both on the waveform and spectrum. The simulation results show that the distortion of RF introduces a variable noise figure to the transceiver in different input signal level. The increased input will introduce more distortion according to the non-linear effects in RF components. The comparison of the simulation result and Welkin design goal shows that it meets the goal and reflects the effect of noise figure and receiver sensitivity correctly. The signal feature in each stage from this simulation can be used as a reference for hardware testing. The integration with Matlab custom tokens also indicates the possibility of a multi-domain simulation methodology to apply different capabilities of various platforms.

By far, the platform doesn't include the carrier recovery and the bit-synchronization modulo. However, in the real system, carrier recovery and synchronization are two key techniques to make the system work properly. As these schemes are done in the digital part, we need to study the DSP/FPGA implementation techniques. I am now studying AFC/DPLL schemes.

The radio implementation of the PHY for IEEE 802.11 standard specifies the use of either Frequency-Hopping Spread Spectrum (FHSS) or Direct Sequence Spread Spectrum (DSSS) modulation. For FH radios the IEEE specifies a minimum requirement of 1 Mbps data rate using two-level Gaussian frequency shift keying (2GFSK) modulation. An optional rate of 2 Mbps is supported using four-level Gaussian FSK (4GFSK) modulation.

Another modulation technique known as M-ary Biorthogonal Keying (MBOK) has been used to achieve a 5.5X improvement in data transmission rate when compared with that for DQPSK, and radios utilizing the MBOK modulation format have now achieved FCC certification. This can be a long-term direction for higher data rate implementation.

In this simulation we only simulated the scheme for single user. Next we may try to simulate multi-user schemes.

Combined with our current considerations, future directions for this work could be:

(1). Integrate with the current W-CDMA testbed to support multi-user detection and estimation;

(2). Design/look for controller card for RF interface;

(3). Test the welkin RF hardware and design the baseband interface;

(4). Integrate the SystemView simulation with current CDMA testbed in Simulink and TI DSP;

(5). Try other more complicated modulation schemes in baseband: OFDM, QAM, MPSK, GFSK, MBOK;

(6). Insert channel coding schemes;

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