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Meniscus-Mask Lithography for Fabrication of Narrow Nanowires

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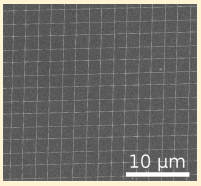
Supporting Information

ABSTRACT: We demonstrate the efficiency of meniscus-mask lithography (MML) for fabrication of precisely positioned nanowires in a variety of materials. Si, SiO_2, Au, Cr, W, Ti, TiO_2, and Al nanowires are fabricated and characterized. The average widths, depending on the materials, range from 6 to 16 nm. A broad range of materials and etching processes are used and the generality of approach suggests the applicability of MML to a majority of materials used in modern planar technology. High reproducibility of the MML method is shown and some fabrication issues specific to MML are addressed. Crossbar structures produced by MML demonstrate that junctions of nanowires could be fabricated as well, providing the building blocks required for fabrication of nanowire structures of varied planar geometry.



Narrow metallic and semiconducting wires are important for purposes of miniaturization, addressing ultrasmall devices, and for exploiting properties of materials arising from spatial confinement such as band structure distortions and conductivity quantization.[1−3] Current nanowire fabrication methods can be divided into two major groups: bulk synthesis or lithographic. Bulk methods[1,4−6] allow for the synthesis of large quantities of individual nanowires, with control over their crystallinity and sometimes even crystallographic orientation. However, as there is no facile method to position an array of these wires on an integrated circuit plane, bulk synthetic methods are not suitable for integration into the modern planar technology used by the semiconductor industry.[1,7−11] In contrast, lithographical methods are widely used in industrial processes, but the resolution of conventional lithography is limited by the lithographic tool and resists, and making very fine features can be exceedingly costly.[12−14] Even though narrow nanowires can be fabricated by fine-tuned electron beam lithography,[14−16] doing this en masse is difficult.[14,17]

A separate approach implemented, for example, in a sidewall image transfer technique,[17−19] uses deposition of the mask on the sidewall of some pattern, as it gives precise control over the resulting nanowire width. Modern film deposition methods such as atomic layer deposition allow for control over the film thickness within a single atomic layer. However, deposition of material onto closely located sidewalls could be difficult due to shadowing and capillary effects.[20−22] Meniscus-mask lithography (MML) was shown for the fabrication of graphene nanoribbons.[23] This method is based on projection of either electron-beam or photolithography patterned sidewalls using adsorbed water as the mask. In this paper, we extend MML to a wide variety of metals, metal oxides, and semiconductors and further demonstrate that more complex structures, such as junctions and crossbars, can be fabricated. A particular advantage of the MML method is precise positioning of narrow nanowires that is required for large-scale device fabrication. The process could be directly integrated into modern planar technology with no modifications to existing equipment and minimal changes in fabrication protocols. No new tools or materials are required.

The general process scheme resembles the one described previously[23] and is schematically represented in Figure 1A. In a typical process a thin film of target material is covered with resist film (step 1) and patterned so that the edges of the pattern are located at the designated nanowire positions (step 2). Then, directional dry etching is performed (step 3) in order

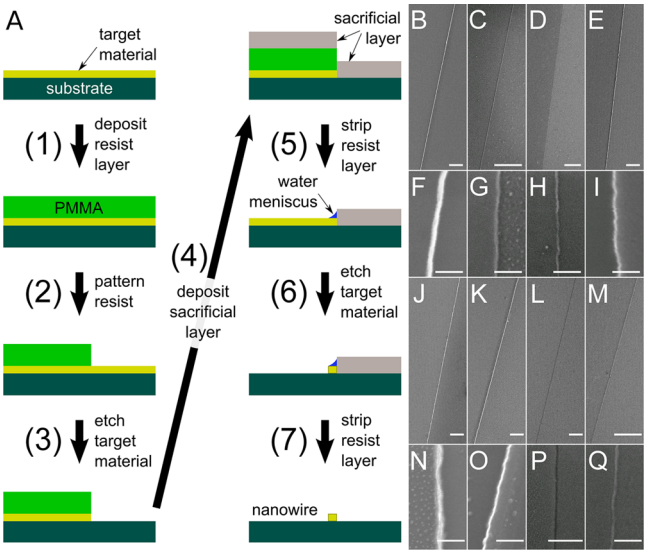


Figure 1. MML fabrication of wires. (A) MML fabrication scheme. Examples of wires at low and high magnification SEM images: (B, F) Si wires; (C, G) SiO_2 wires; (D, H) Au wires; (E, I) Cr wires; (J, N) W wires; (K, O) Ti wires; (L, P) TiO_2 wires; (M, Q) Al wires. The scale bars for images (B−E) and (J−M) are 1 μm and for images (F−I) and (N−Q) are 100 nm.

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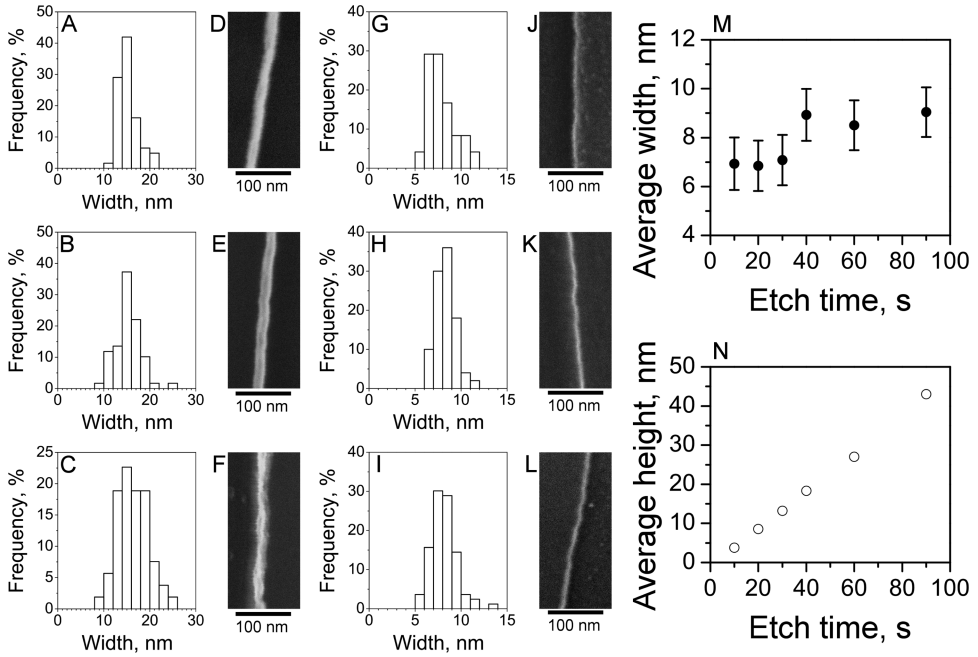

Figure 2. Si and SiO_2 model wires produced with MML. (A–F) Width distribution and typical SEM images of Si wires fabricated with (A, D) Ar/Cl_2 etching, (B, E) HBr/Cl_2 etching, and (C, F) SF_6/O_2 etching. (G–L) Width distribution and typical SEM images of SiO_2 wires fabricated with (G, J) CHF_3/O_2 etching, (H, K) CF_4/O_2 etching, and (I, L) SF_6/O_2 etching. (M–N) Variation of SiO_2 (M) wires width and (N) height with etching time for SF_6/O_2 etching.

to remove material exposed through the lithographic pattern. After that, the sacrificial metal layer is deposited (step 4) and the resist layer is stripped (step 5). Finally, a second directional dry etching is performed (step 6) and the material exposed through the sacrificial metal layer mask is etched, and then the sacrificial metal mask is wet etched (step 7). During the second dry etching (step 6), the narrow region nearby the sacrificial metal mask is protected by a thin adsorbed water layer, which is slightly thicker nearby the wedge,[23] resulting in consistent formation of long, narrow, precisely positioned nanowires of the target material. The contact area of water depends on the target material. Hydrophobic materials, such as the PMMA resist layer, do not form a meniscus.

The MML process could be used to fabricate the wires out of a number of materials (Figure 1). We have successfully prepared Si wires (Figure 1B,F), SiO_2 wires (Figure 1C,G), Au wires (Figure 1D,H) with an average width of 7.0 ± 1.0 nm, Cr wires (Figure 1E,I) with an average width of 11.4 ± 1.0 nm, W wires (Figure 1J,N) with an average width of 15.9 ± 1.0 nm, Ti wires (Figure 1K,O) with an average width of 9.8 ± 1.0 nm, TiO_2 wires (Figure 1L,P) with an average width of 10.9 ± 1.0 nm, and Al wires (Figure 1M,Q) with an average width of 6.9 ± 1.0 nm. Additionally, we previously reported similar fabrication of Pt wires (average width 11.7 ± 1.0 nm).[23] The Si wires are presented in detail in Figure 2 and the resulting discussion. The etching conditions utilized and other fabrication details are summarized in Supporting Information Tables S1–S3. The distributions of wire widths are shown in Supporting Information Figure S1, and detailed statistical parameters of resulting wires are summarized in Supporting Information Table S4. Typical AFM images of MML fabricated nanowires are shown in Supporting Information Figure S2. The nanowires' height is uniform over their length and is equal to or slightly exceeding the thickness of the starting target material film.

In order to demonstrate the versatility of the MML fabrication method, we have thoroughly analyzed the critical process step, the dry etching, demonstrating the water meniscus mask stability against different types of plasma processes. Reactive ion etching (RIE) is a conventionally accepted term for all plasma etching processes; however, there are several different phenomena occurring in plasma discharges leading to materials etching: (1) physical sputtering when the target material gets removed from the substrate due to bombardment with highly energetic ions, (2) chemical etching when plasma species react with the target material on their own, (3) ion-enhanced energetic etching when plasma species react with the substrate only if sufficiently accelerated toward it, and (4) ion-enhanced inhibitor etching when plasma species cause the formation of a protective inhibitor layer everywhere except the areas exposed to ion flux.[24] All of those mechanisms are directional except chemical etching, which works isotropically. Methods relying solely on physical sputtering are easily distinguishable from chemically assisted directional plasma etching. However, ion-enhanced energetic and ion-enhanced inhibitor mechanisms typically coexist in directional dry etching processes.

The typical example of physical sputtering removal of material is etching of noble metals (Au, Pt) with Ar plasma. Sputtering works on diverse materials, however, the typical etch rates are low,[24] and other etching processes are usually preferred for chemically active materials. Redeposition is a common problem for physical sputtering and occurs when sputtered substrate atoms/clusters are not removed from the system but return to the substrate or stick to the mask walls.[25,26] Although we successfully fabricated narrow Au and Pt wires in the MML process, their yield was limited by random formation of much thicker irregular objects (Supporting Information Figure S3), which we attributed to redeposition effects. The size of those objects suggests they were mostly

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formed during the first etching step, and indeed we were able to mitigate this problem by adjusting the lithography conditions to make the PMMA sidewall slope outward enabling better removal of sputtered material.

Unlike sputtering, which is always directional, the chemically assisted dry etching processes are characterized both by the etch rate and the undercut, which is the relative impact of isotropic etching, that is, the etching that occurs in a direction parallel to the substrate. For MML fabrication of narrow wires, highly directional processes are desired, as the undercut affects the width of the resulting wires up to their complete disappearance. Unlike the exact process mechanism, undercutting is well documented for different plasma etching processes. Preferred compositions of plasma are well known for various materials. For example, fluorine-based plasmas are widely used to etch Si (refs 27 and 28), SiO_2 (refs 29 and 30), W (ref 31), Ti (ref 32), and TiO_2 (ref 33), whereas chlorine-based plasmas are used for etching of Si (refs 27, 28, and 34), W (ref 17), Al (ref 35), and Cr (ref 36). We have found that wire formation occurs independent of the exact directional etching mechanism for all those systems (Figure 1).

In some particularly aggressive plasmas, such as Cl_2/O_2 or $Cl_2/O_2/N_2$ etching of Cr, and Cl_2/Ar etching of W, the important issue of resist erosion[37] manifested itself in the formation of shelf-like structures adjacent to the wire (Supporting Information Figure S4). It is observed on the side of the wire exposed in the first etching step and could not be avoided simply by increasing the first etching time. We were able to ameliorate this effect by adding a physical sputtering step immediately after the first etching step, as sputtering does not withdraw the resist edge and removes residuals of exposed metal that otherwise would form the shelf.

In order to compare the effect of different etching methods on nanowire formation, we used Si and SiO_2 as model systems. The etching of these materials is well studied; they are readily available commercially in the form of silicon-on-insulator and thermal SiO_2 coated Si wafers and they have smooth uniform surfaces.

Figure 2A–F shows the width distributions and corresponding typical SEM images of Si wires prepared with different etching processes. The average width of Si wires is 15.2 ± 1.0 nm for Ar/Cl_2 etching, 15.4 ± 1.1 nm for HBr/Cl_2 etching, and 16.4 ± 1.1 nm for SF_6/O_2 etching. In the Ar/Cl_2 process, an impenetrable nonvolatile layer of $SiCl_x$ is formed on the Si surface, and the directional process results from argon ion bombardment volatilizing $SiCl_x$ from the bottom.[24,27] The process of HBr/Cl_2 etching is similar, but the passivating layer contains Br as well.[27] In the SF_6/O_2 process, the SiO_xF_y film is sputtered from the bottom and redeposited on the sidewalls resulting in directionality etching.[24,27,28] For the SF_6/O_2 etching procedure, we measured a wider wire width distribution than for other procedures; however, the average wire widths for all three etching methods are very close, indicating that the exact etching mechanism or chemistry involved do not significantly affect the result.

Figure 2G–L shows the width distributions and corresponding typical SEM images for SiO_2 wires prepared with different etching processes and in different etching instruments. The average width of SiO_2 wires is 7.9 ± 1.0 nm for CHF_3/O_2 etching, 8.3 ± 1.0 nm for CF_4/O_2 etching, and 8.0 ± 1.0 nm for SF_6/O_2 etching. All three processes result in formation of passivating layers on the walls of etched trenches; however, the composition of these passivating layers is different.[17,28] Also, the CHF_3/O_2 and CF_4/O_2 processes work through formation of a fluorocarbon film on the etched plane,[17] whereas the SF_6/O_2 process depends mostly on fluorine reactivity.[24,28] The width distributions of wires fabricated using those different processes, however, are similar. Moreover, these results were reproduced in four different RIE instruments, thereby exemplifying the method reproducibility.

For the SF_6/O_2 etching process, we have tested the wire cross section evolution with etching time. Figure 2M shows the average width of the wires, which do not change significantly, and Figure 2N shows the average height of the wires, which increases linearly with etching time. This suggests that the water mask is sufficiently stable to provide wires of arbitrary height over a wide range. This formation of arbitrary height wires comes with certain requirements: (1) the etching procedure needs to be adjusted so as not to damage the resist or sacrificial metal mask before the desired etch depth is achieved and (2) the process undercut is minimal.

In order to verify the apparent continuity of the wires and to characterize their electronic transport behavior, we patterned leads onto the wires (Supporting Information Figures S5–S7). Most types of wires (Au, Ti, Cr, W, Si) were conductive, and Si wires were operating as FET devices when backgated by the handling Si layer (Supporting Information Figure S7). However, for native oxide forming metals (Ti, Cr, W), the conductivity was several orders of magnitude lower than expected, which could originate from oxidation of the outer wire region. Al wires were found to be nonconductive, most probably for the same reason.

The fabrication method that we demonstrated here permits not only arbitrary shaped individual wires or parallel arrays of those, but also crossbars of wires, both homogeneous with the same material wires intersecting (Figure 3A), and heteroge-

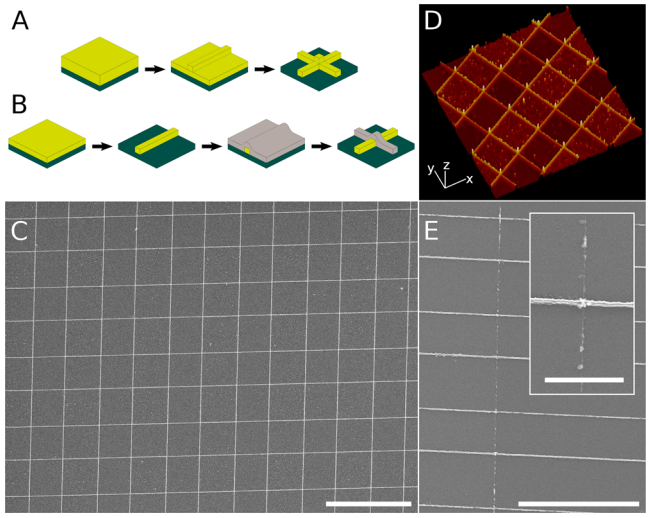

Figure 3. Crossbar structures prepared with MML. (A–B) Schematics of crossbar structure fabrication for (A) homogeneous (both wires are made out of the same material) and (B) heterogeneous (wires are made of different materials) crossbars. (C) SEM image of homogeneous SiO_2–SiO_2 crossbars. Scale bar is 5 μm. (D) AFM image of homogeneous SiO_2 crossbars. Scale bars are (x) 1 μm, (y) 1 μm, (z) 125 nm. (E) SEM image of heterogeneous Si–Pt crossbar structure (Si horizontal, Pt vertical). Scale bar is 5 μm. Inset: magnified image of individual wire intersection. Note that bright speckles on Pt wire are traces of redeposition; the actual Pt wire is a thin vertical line on the image (see text). Scale bar is 1 μm.

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neous with different wire materials wires intersecting (Figure 3B). SiO_2/SiO_2 homogeneous crossbar structures (Figure 3C,D and Supporting Information Figure S8) were prepared by repeating the same MML fabrication sequence twice, one pattern array perpendicular to another. The magnified image of the intersection site (Supporting Information Figure S8A inset) shows that intersecting wires are connected. The AFM image (Figure 3D and Supporting Information Figure S8B,C) shows that both wires have approximately the same height, and the intersection point is elevated by the height of one wire over another wire, thus twice that elevated over the bottom of the chip. The structure could also be interpreted as a regular array of narrow tips. A Si/Pt heterogeneous crossbar structure (Figure 3E) was prepared by depositing Pt onto an array of MML fabricated nanowires and repeating the MML procedure with a pattern perpendicular to the Si wires. Bright speckles on Pt wire are traces of redeposition, which was significant here in both etching steps of Pt wire preparation, as the Si wires height is ~100 nm; the actual Pt wire is a thin vertical line on the image.

In conclusion, we demonstrated that the MML approach is suitable for the fabrication of narrow nanowires from Si, SiO_2, Au, Cr, W, Ti, TiO_2, Al. A range of materials and etching processes suggest the applicability of MML to a wide array of materials used in modern planar technology. We also discussed some fabrication difficulties specific to materials and processes used and demonstrated that they could be avoided. Crossbar structures show that junctions of nanowires could also be fabricated. Thus, MML provides the building blocks required for fabrication of a host of nanowire structures over various geometries.

Methods. Metal wire samples were made using polished, single-sided, heavily p-doped Si wafers with a 300 nm thermal SiO_2 layer (Silicon Quest International) as substrates. Starting metal films were deposited onto substrates via sputtering (Denton Desk V Sputter system) or e-beam evaporation. These Si/SiO_2 substrates were also used as a starting film in preparation of SiO_2 nanowires. Silicon on insulator (SOI) wafers with a 100 nm p-doped ⟨100⟩ oriented device layer (resistivity 8.5−11.5 Ω·cm), a 200 nm oxide layer and a 500 μm heavily p-doped handling layer were used as a starting material for Si nanowire fabrication. TiO_2 films were deposited on Si/SiO_2 wafers using an atomic layer deposition system (courtesy of Dr. M. Thomas and Dr. P. J. Joseph, Georgia Tech University). Electron-beam lithography patterning and SEM imaging were performed using a JEOL 6500F scanning electron microscope. Images were acquired at a 15 kV accelerating voltage in SE mode with no additional conductive coating applied. Lithography patterns were written using PMMA 950 A resist at 30 kV accelerating voltage and 300 pA beam current. Reactive ion etching was performed using a Trion RIE instrument, Oxford RIE 80 instrument, Oxford ICP 100 instrument and 790 Plasma Therm RIE instrument. A detailed description of etching conditions is given in the Supporting Information section.

■ ASSOCIATED CONTENT

Supporting Information

Further details are provided on fabrication procedures, statistical analysis of nanowire width distributions, defects caused by material redeposition and mask erosion, and nanowires' conductivity. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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