DSP for Embedded and Real-Time Systems

Expert Guide

Robert Oshana

CHAPTER 8

High-level Design Tools for Complex DSP Applications

Yang Sun[1], Guohui Wang[1], Bei Yin[1], Joseph R. Cavallaro[1], Tai Ly[2]

[1]Rice University, ECE Department, Houston, TX [2]National Instruments Corporation, Austin, TX

High-level synthesis design methodology

High level synthesis (HLS) [1], also known as behavioral synthesis and algorithmic synthesis, is a design process in which a high level, functional description of a design is automatically compiled into a RTL implementation that meets certain user specified design constraints. The HLS design description is 'high level' compared to RTL in two aspects: design abstraction, and specification language.

DSP for Embedded and Real-Time Systems. DOI: 10.1016/B978-0-12-386535-9.00008-1