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Resistive Switching and Memory Effects in Silicon Oxide Based Nanostructures

by

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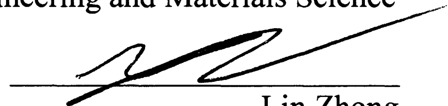

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ABSTRACT

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Silicon oxide (SiO_x, $1 < x \leqq 2$) has long been used and considered as a passive and insulating component in the construction of electronic devices. In contrast, here the active role of SiO_x in constructing a type of resistive switching memory is studied. From electrode-independent electrical behaviors to the visualization of the conducting filament inside the SiO_x matrix, the intrinsic switching picture in SiO_x is gradually revealed.

The thesis starts with the introduction of some similar phenomenological switching behaviors in different electronic structures (Chapter 1), and then generalizes the electrode-material-independent electrical behaviors on SiO_x substrates, providing indirect evidence to the intrinsic SiO_x switching (Chapter 2). From planar nanogap systems to vertical sandwiched structures, Chapter 3 further discusses the switching behaviors and properties in SiO_x. By localization of the switching site, the conducting filament in SiO_x is visualized under transmission electron microscope using both static and *in situ* imaging methods (Chapter 4). With the intrinsic conduction and switching in SiO_x largely revealed, Chapter 5 discusses its impact and implications to the molecular electronics and nanoelectronics where SiO_x is constantly used. As comparison, another type of memory effect in semiconductors (carbon nanotubes) based on charge trapping at the semiconductor/SiO_x interface is discussed (Chapter 6).

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Table of Contents

Title Page i

Abstract ii

Acknowledgements iii

Table of Contents v

1. Introduction and Backgrounds

1.1 What is Resistive Switching Memory and Why Pursue it? 1

1.2 Classification of Resistive Switching Memory

1.2-1 Classification Based on Phenomenological Behavior 5

1.2-2 Classification Based on Mechanism....7

1.3 Resistive Switching in Low-Dimensional Nanomaterials 9

1.4 Implications 13

2. Resistive Switching in Planar Nanogap Systems on SiO_x ($x \sim 2$) Substrates

— An Electrode-Independent Switching Scenario

2.1 Motivation and Outline 16

2.2 Resistive Switching in Various Nanogaps

2.2-1 Lithography-Defined Metal-Metal Nanogap 17

2.2-2 Amorphous-Carbon Nanogap System 21

2.2-3 Titanium Nitride Nanogap 26

2.2-4 Nanogaps Formed by Metal Islands 27

2.2-5 Nanogaps by Multi-Walled Carbon Nanotubes 29

2.2-6 Nanogaps by Single-Walled Carbon Nanotubes 33

2.3 Mechanism Discussions 36

2.4 Summary 39

3. Resistive Switching in SiO_x in Vertical Representations

3.1 From a Planar Structure to a Vertical 42

3.2 Resistive Switching in Vertical SiO_x with Metal Electrodes

3.2-1 Fabrication 43

3.2-2 Characteristic *IV* Curves and Memory Switching 45

3.2-3 Electroforming and Its Implication 48

3.2-4 Summary 56

3.3 Resistive Switching in Metal-Free polySi-SiO_x-polySi Structures

3.3-1 Fabrication 58

3.3-2 Memory Switching and *IV* Curves 59

3.3-3 Metal-Free Fabrication Process 61

3.3-4 Forming Processes and Implications 63

3.3-5 Protrusion and Pore Structures 69

3.4 Memory Properties

3.4-1 Retention 73

3.4-2 Thermal-Annealing Effects on the Memory State 77

3.4-3 X-Ray and Heavy-Ion Irradiation Tests 82

3.4-4 BOE Etching Test 85

3.4-5 Switching Speed 87

3.4-6 Memory Endurance 91

3.5 Summary 94

4. Probing the Conducting Filament in SiO_x Memory Devices and Mechanistic Implication

4.1 Static TEM Imaging of the Filament

4.1-1 Locating and Visualizing the Filament 98

4.1-2 The Proposed Mechanistic Picture 102

4.2 *in situ* Imaging of the Filament

4.2-1 Challenge and Opportunity 108

4.2-2 Device Design and Fabrication 110

4.2-3 *in situ* Imaging 116

4.3 Summary 128

5. SiO_x is a Non-Innocent Substrate in Molecular Electronics and Nanoelectronics Studies

5.1 Introduction 131

5.2 Main Discussion

5.2-1Molecular Effect? 133

5.2-2 SiO_x Related Non-Linear Behaviors 137

5.2-3 Material-Assisted Forming 144

5.2-4 NDR and Current Hysteresis at Low Voltage 151

5.3 Summary 157

6. Memory Effect in Single-Walled Carbon Nanotubes: Charge Trap at the SiO_x/Carbon-Nanotube Interface

6.1 Introduction 159

6.2 Results and Discussion

6.2-1Hysteresis and Memory Effect ...160

6.2-2 Mechanism Discussion ...163

6.2-3 Charg-Based Current Hysteresis in Other Materials ...171

6.3 Summary ...173

7. List of References ...174

8. Appendix ...189

1. Introductions and Background

1.1 What is Resistive Switching Memory and Why Pursue it?

The ever-increasing demand for portable electronic devices has made flash memory the fastest growing type of memory[1] (see Fig. 1). Some even predicted that flash memory would replace hard disks in some ultra-light notebook or tablet computers.[2] Nevertheless, a miniaturization limit is projected as the industry moves toward memory cells with 22-nm lateral width in 2016.[3,4] The main reason is that, for a charge-storage based memory, it becomes increasingly difficult to reliably control or retain electrons in the shrinking dimensions.[3] Although new technology such as the multilevel cell (MLC)[2] eases the problem to a point, common challenges such as short-channel effects or gate tunneling remain.[1]

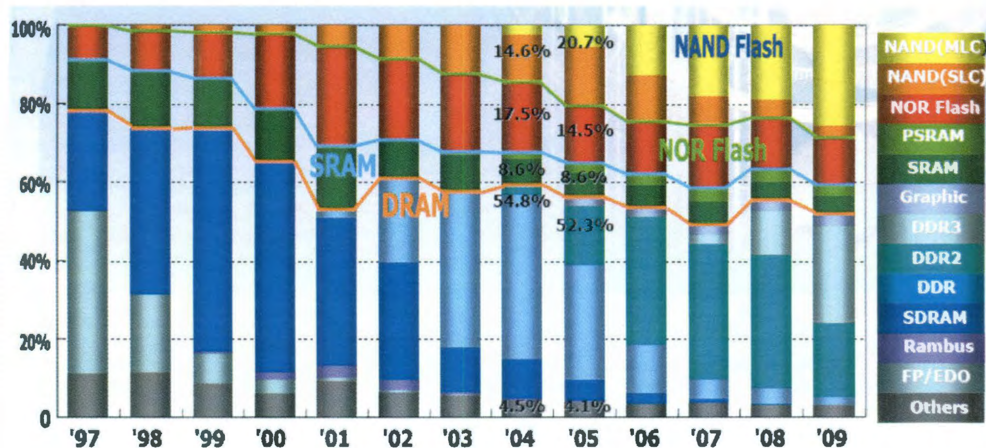


Figure 1. Memory Market Trend (Revenue Based) (Source: Dataquest, Semico, iSuppli, Samsung). URL: www.itrs.net/Links/2007ITRS/ExecSum2007.pdf.

Regarding the limit in conventional device scaling (*e.g.*, simply making the transistor smaller), various concepts and studies in fields such as molecular electronics[5-8] and spintronics[9-11] have been pursued as potential replacements for flash. One of the promising candidates is resistive switching memory[12,13] based on resistance-change materials (RCMs),[3] in which the RCM is usually sandwiched between two electrodes, serving as the basic memory unit (see Fig. 2a for illustration). During the programming process, electrical stress (voltage/current) is applied on the RCM between the two electrodes. The conductance of the RCM can be altered according to the amount of electrical stress applied. The change of the conductance is usually larger than 1000%, with the RCM retaining its conductance even when it is unbiased. Therefore, a memory unit in a two-terminal configuration, instead of using three-terminals as used in transistors in conventional flash memory, can be constructed. For example, the low-conductance (OFF) and high-conductance (ON) states can be read as binary states of "0" and "1" for data storage. For addressable memory arrays, a crossbar structure (in conjunction with diodes) is usually adopted (Fig. 2b).

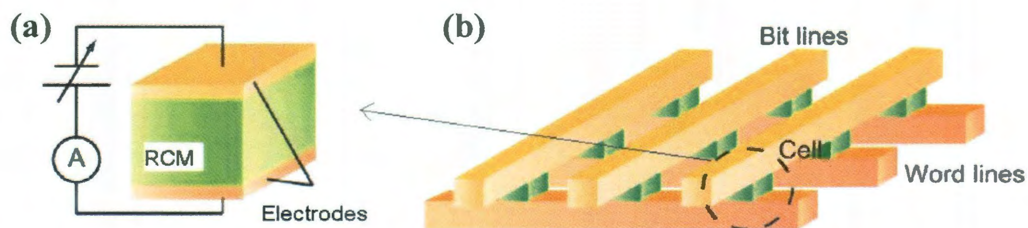


Figure 2. (a) Illustration of RCM material sandwiched between two electrodes as the

basic memory unit, in which electrical stress (voltage or current) is applied between two electrodes. (b) A schematic of memory array based on crossbar structure (a diode is needed for each memory unit at one of the RCM/electrode interfaces, but is not shown in this illustration). Graphics are reproductions from Ref. [12].

Compared to flash memory, resistive switching memory features the following advantages: (1) It is non charge-based. Both phase-change and programmable metallization memory (discuss later) appear to promise much extended scaling without losing the device functionality. For example, in programmable metallization memory, researchers demonstrated that a metallic bridge can be scaled controllably to 0.5 nm.[14] (2) Simpler structure. The two-terminal configuration enables simpler memory architecture. In other words, it takes up less space and the fabrication cost to construct the same number of memory units is less, producing higher memory density and lower storage price. The two-terminal resistor-like structure in a way promises an easier multilevel-stacking scheme to construct 3-D memory.[13] (3) Fast switching time. The process of charge-and-discharge through a gate oxide in flash memory limits the switching time to > μs. The switching in RCMs can be several ns,[3,15] making it a much faster memory.

Despite of the above promising features for nonvolatile memory, resistive switching memory has certain disadvantages: (1) Reliability concerns. For flash memory, a minimum memory endurance (memory cycles) of 10^4 and data storage

time of ~ 10 years are common specification. Although memory cycles as high as 10^6 have been demonstrated,[16] with an extrapolated data retention time over 10 years,[17-19] insufficient data is provided concerning device uniformity (device yield and variations).[12] (b) Power consumption concerns. The programming current in a float-gate memory unit in flash memory is < nA since the current is mainly by tunneling through the SiO_2 layer to charge/discharge the unit. For most resistive switching memory, this current is > μA. The high programming current counteracts the fast switching time as power consumption is proportional to the product of both. While optimization in architecture or software can ease the problem of comparatively slow programming in flash memory to achieve higher speed, no such rule could be applied when it comes to power consumption, from which heat dissipation will in turn prevent the fabrication of denser memory.

These pros and cons of resistive switching memory have stimulated a great interest in the field of RCM since the 1960s and more advances are likely to be made, given the huge economic stake involved; the memory market in 2007 was $60 billon with flash memory representing one third of the total. On the other hand, the switching mechanisms in various RCMs are dependent upon more advanced understandings in physics, chemistry and materials science, which have yet to be sufficiently delineated.

1.2 Classification of Resistive Switching Memory

1.2-1 Classification Based on Phenomenological Behavior

Usually, resistive switching memory can be classified into two categories. From the phenomenological behavior or current-voltage (*IV*) evolutions, the switching in RCMs is either unipolar (nonpolar) or bipolar.

In unipolar switching, the change in resistance depends on the amplitude of applied voltage but not on the polarity (*e.g.*, whether it is positively or negatively biased). Because of the nonpolarity dependence, the switching is likely to be Joule heating related.[13] Most pristine RCMs are insulating or semiconducting; high voltage is needed to initialize the RCMs into switching states, which is referred to as the electroforming process.[20] In the electroformed device, as shown by green and grey curves in Fig. 3a, the ON state can be changed into an OFF state by sweeping to a certain voltage (threshold "reset" voltage). As shown by the red curves in Fig. 3b, the change from an OFF state to an ON state involves another threshold voltage ("set" voltage). Since the reset process (from ON to OFF) is likely to be Joule-heat-related breaking of the conducting paths, a current compliance (CC) is usually needed for the set process (indicated by the red dashed curves in Fig. 3a). These two processes are symmetric in both positive and negative voltage bias regions as shown in Fig. 3a. By applying voltages (pulses) of different amplitudes, for example, at the set/reset threshold voltage, the conduction (memory) state of the material can be "written"/"erased" to correspond to the ON/OFF state. This type of switching is

observed in highly insulating oxides, such as NiO,[21] Al_xO_y,[22] ZnO,[23] ZrO,[24] and SiO,[20] with the set voltage value not necessarily larger than the reset one.[25]

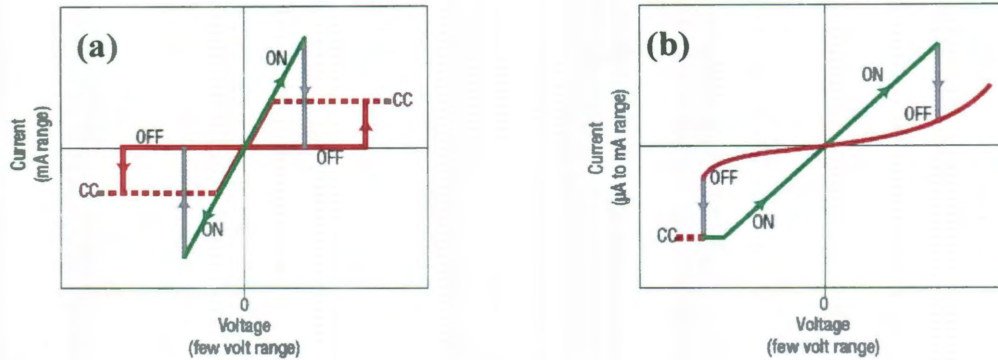


Figure 3. (a) *IV* evolutions in a unipolar switching memory. The arrows indicate the voltage sweep directions. "CC" means a current compliance. (b) *IV* evolutions in a bipolar switching RCM. Graphics are reproductions from Ref. [13].

In the other type of bipolar switching, the change of resistance is polarity dependent. Usually a threshold voltage value in a given polarity sets the material from an OFF state into an ON state (left side in Fig. 3b), whereas a threshold voltage value (not necessarily having the same amplitudes) in the opposite polarity resets the ON state into the OFF state (see right side in Fig. 3b). This type of switching behavior is usually observed in semiconducting oxides, such as complex perovskite oxides.[12,26-28] Some materials, such as TiO_x[29] and Cu-doped SiO_2[30] can show both unipolar and bipolar switching behaviors.

1.2-2 Classification Based on Mechanism.

Based on the switching mechanism, resistive switching memory can be categorized[3] as (i) phase-change memory, (ii) programmable-metallization (metal-filament based) memory or (iii) metal-oxide (oxygen-vacancy based) memory.[13]

Phase-change memory relies on a resistance change between the ordered crystalline state and a disordered amorphous form[3,31] (left images in Fig. 4). The transition between these two states is triggered by electrical heating through an applied voltage bias. Depending on the amplitude and duration of the electrical signal applied, the material can solidify into a crystalline low-resistance state or into an amorphous high-resistance state. For example, in $Ge_2Sb_2Te_5$, a pulse heating (~ 10 ns) above the melting temperature (~ 600 ^{o}C) with subsequent rapid cooling (~10^9 K s^{-1}) produces amorphous material, while longer heating (*e.g.*, 100 ns) below the melting temperature leads to recrystallization.[32] A majority of phase-change materials are derived from the chalcogenides such as $Ge_2Sb_2Te_5$, GeTe[33] and SbTe.[34]

Programmable metallization memory is based on mobile metal ions embedded in a solid electrolyte glass matrix[3] (middle images in Fig. 4). Usually a metal ion reduction-oxidization (redox) electrochemical process is believed to be responsible for the switching, in which the creation or annihilation of a nanoscale metallic conducting path (metal filament) results in the ON or OFF state. Since the

electrochemical redox process is polarity dependent, this type of memory usually has a bipolar switching behavior. Included in this category are metal doped systems[13] such as Ag_2S,[35] CuS[36] and Cu-doped SiO_2.[30]

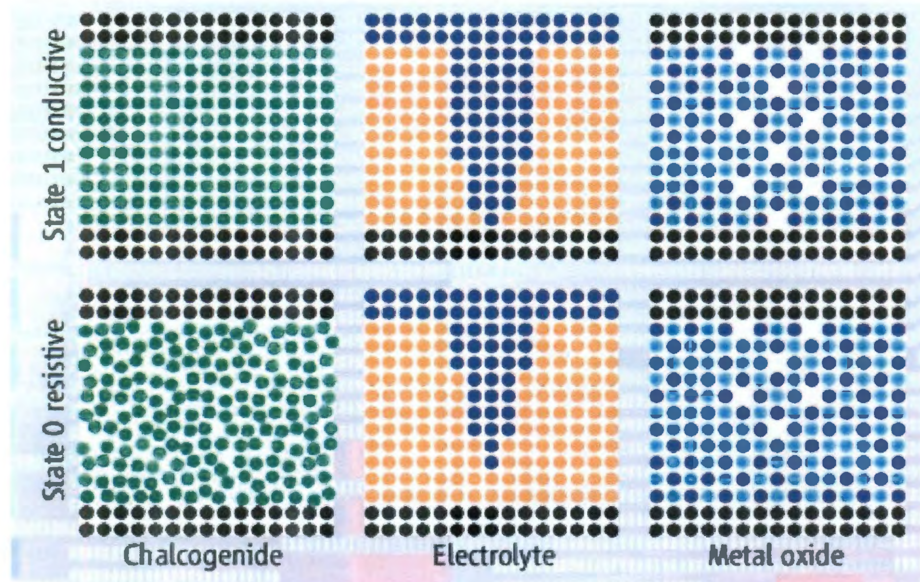


Figure 4. Resistance-change memory concepts: (Left) Crystalline and amorphous states in phase-change materials. (Middle) Creation and annihilation of a metal filament path in programmable metallization memory. (Right) Creation and disruption of a path of missing oxygen atoms in a transition-metal oxide. Figures are reproductions from Ref. [3].

Oxygen vacancies are considered to be the cause in resistive switching observed in various transition metal oxides, ranging from perovskites such as $SrTiO_3$ to binary oxides such as NiO. Although not yet fully understood, the movement of oxygen vacancies, particularly at the vicinity of the electrode/material interface,[12] modulates the valence of the transition-metal ions (*e.g.*, between Ti^{3+} and Ti^{4+} in TiO_x) and thus

the conducting state[3] (right images in Figure 4). Studies[13,37] showed that this type of switching is similar to programmable metallization memory in that the switching is largely through filamentary conduction.

1.3 Resistive Switching in Low-Dimension Nanomaterials

Strictly speaking, modern electronics are mostly based on structures at or approaching the nanoscale. As mentioned above, one of the advantages of resistive switching memory is indeed the possibility of extended scaling to sub 100 nm. At this scale, any of the memory structures fabricated by standard lithographic technology would be considered as nanomaterials.[38] However, to a point, nature has the preference of assembling small structures from the bottom-up, a process that top-down methods may not be able to reproduce. Among them, materials such as fullerenes[39] and carbon nanotubes (CNTs)[40] are examples that are considered as new forms of carbon. Due to their self-constricted and highly-ordered crystalline structures, these materials are referred as 0-D or 1-D systems.[41] In a similar way, various nanowires[42] grown from the bottom-up, though often not as ordered as fullerenes or CNTs in regard to their crystalline structure, particularly at the surface, are also considered as quasi-1D structures due to the high aspect ration between their length and diameter.[43] The discovery of graphene (single or a few layers of graphite sheets),[44] on the other hand, leads to strictly defined 2-D materials.

Those quasi 1-D or 2-D nanomaterials, with small but highly-ordered structures, have been found to have new/enhanced functions[45] and serve as proof-of-concepts for

future device miniaturization. For example, semiconducting single-walled carbon nanotubes (SWCNTs), with diameters ~ 2 nm, have been found to have transistor properties exceeding those of current Si transistor in some aspects.[46] Similarly, two-terminal memory effects in those nanomaterials have also been found and studied in the hope of identifying future applications.[47-49] On the other hand, the constriction in at least one dimension in those materials is likely to facilitate an easier observation of the memory switching events, thus helping to elucidate the mechanism. The following are three recent examples of resistive switching in quasi 1-D or 2-D materials.

Shown in Fig. 5 is one example in which memory switching behavior was discovered in graphene layers.[47] Initially, the graphene was patterned between two electrodes on a SiO_2 substrate (Fig. 5a left image). Then by voltage sweeping to a high value, electrical breakdown in the graphene layer was induced and a gap feature was produced (right image in Fig. 5a, indicated by two red arrows). Using voltage pulses of different amplitudes of +4 V and +6 V, ON and OFF memory states were programmed, respectively (Fig. 5b). Open-and-break motions in carbon-carbon bonds at the gap region were proposed to be the mechanism (illustration in Fig. 5c). A vacuum environment is reported to be critical for the observed switching behavior.[47]

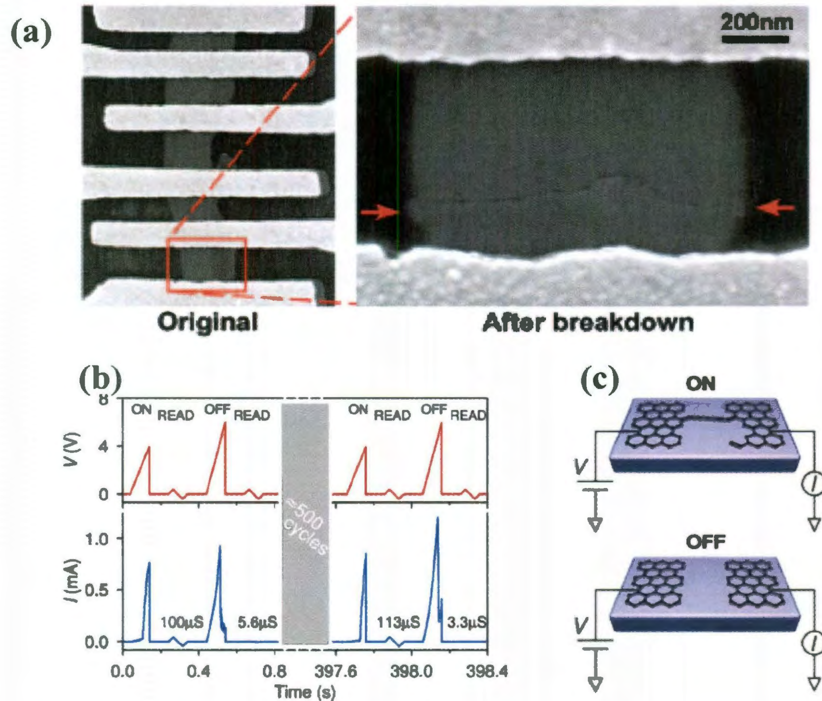


Figure 5. (a) (Left) As-made graphene device and (right) a magnified image after electrical breakdown in the graphene sheet, showing gap feature (indicated by red arrows). (b) Memory programming (cycles) using +4 V and +6 V pulses as writing and erasing voltages, respectively. (c) A schematic of ON/OFF state produced by forming/breaking a carbon-carbon bond. Graphics are reproductions from Ref. [47].

Shown in Fig. 6 is another example showing memory effect in GeTe nanowires (see inset in Fig. 6a) encapsulated by SiO_2 (20 nm thickness).[48] Changes in a void structure were observed during different conduction states (see Fig. 6a and b) and were proposed to be responsible for the memory switching in the GeTe phase-change material. The programming process is similar to that in the graphene device described above, by using voltage pulses of +5 V and +10 V, the nanowire device could be programmed into an ON or OFF state, respectively. The achieved ON/OFF ratio

($\sim 10^7$), however, is higher when compared to the values observed in phase-change materials,[50] and the programming process (*e.g.*, amplitudes of programming voltages) is also different.[51]

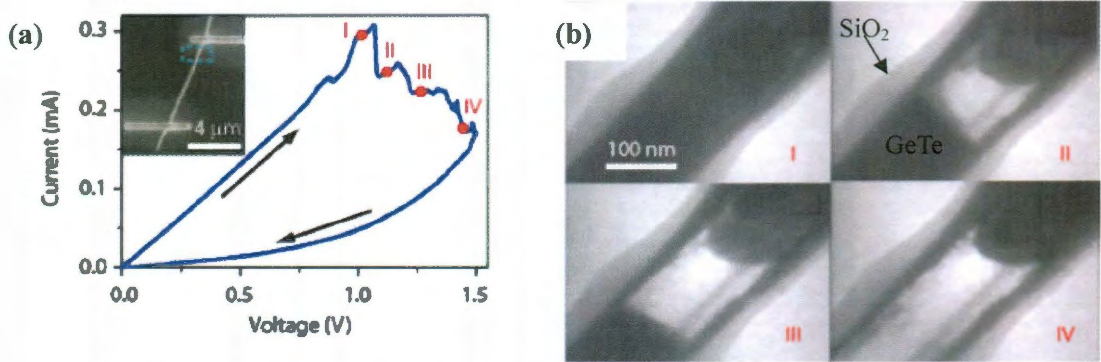


Figure 6. (a) An IV evolution in a GeTe nanowire encapsulated by SiO_2 outer shell, with the inset showing the actual device patterned between two electrodes. (b) A serials of void evolutions with each number corresponding to that indicated in the *IV* curves in (a). Graphics are reproductions from Ref. [48].

Tour's group at Rice University also found resistive switching in nanocable structure,[49] in which the nanocable is a SiO_2 nanowire coated with graphitic layer by chemical vapor deposition (CVD). By sweeping to a high voltage, electrical breakdown in the outer graphitic shell is induced to produce a gap region (Fig. 7a). Memory switching then follows. Again, the switching behavior is similar to that in the previous two systems: by using a set of voltage pulses of +4 V and +8 V, the nanocable can be programmed into ON or OFF state, respectively (Fig. 7b). Electromechanical open-and-break motions of the graphitic layer at the gap region were proposed to be the underlying cause (Fig. 7c for illustration).

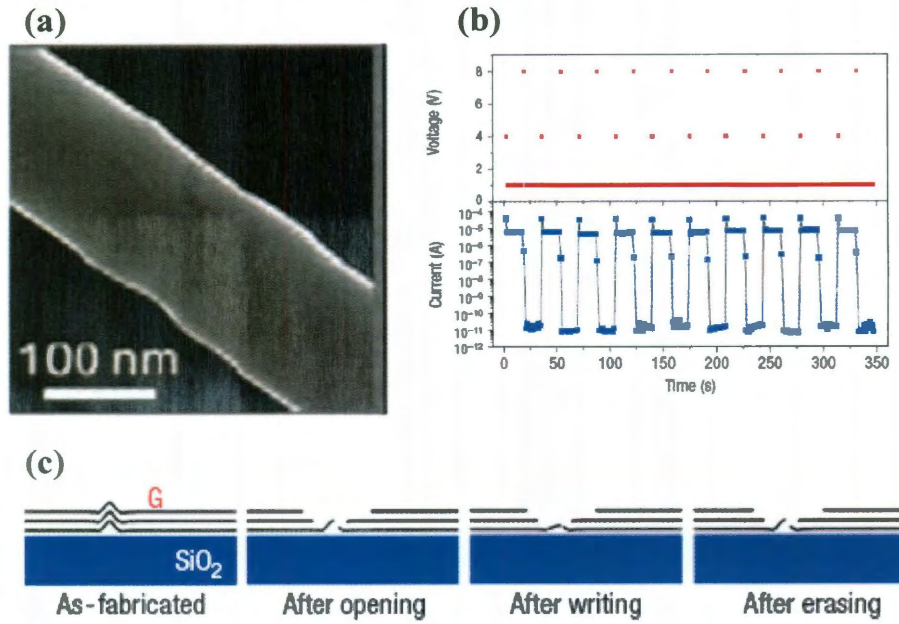


Figure 7. (a) A nanocale that has been subjected to electrical-breakdown, showing the gap feature in the outer graphitic shell. (b) Memory cycles (programming) using +4 V and +8 V as writing and erasing voltages, respectively. (c) A proposed mechanism showing open-and-break motions of the graphitic sheets at the gap region. Graphics are reproductions from Ref. [49].

1.4 Implications

Albeit very different in material compositions and structures, the above resistive switching systems share the similarities in: (1) Gap/void features: a gap (*e.g.*, in graphene and nanocable switching systems) or void region (*e.g.*, in GeTe nanowire) was observed in the conducting layer. (2) SiO_2 as insulating layer: SiO_2 was used as substrate (*e.g.* in graphene), supporting core (*e.g.*, in nanocable), and encapsulating shell (*e.g.*, in GeTe nanowire). (3) Switching behaviors: in all the above devices, a medium voltage, between 3-5 V, was used for a writing operation to set the state from

OFF to ON, while a higher voltage of 6-10 V was used for an erasing operation to set the state from ON to OFF. For the insulating property of SiO_2, it is easily to attribute all the conduction to the conducting material itself. Consequently, the direct observation of gap/void regions in these systems leads to the conclusion that the break-and-rebridge motions of the two broken ends of the conducting material are the cause for the switching.

However, a local high electrical field is built up during programming at the gap/void region, which was largely neglected. Take the nanocable for example. The width of the gap is ~ 10 nm (see Fig. 7a). During an erasing operation using a + 8 V to set the device from ON to OFF, the voltage largely drops at the gap region once an OFF state is obtained. A rough estimate of the local electrical field is 8 V/10 nm or 8 MV/cm, which is close to the breakdown value of most SiO_2.[51] Additionally, there may be some region having the width smaller than 10 nm. Will anything then happen to the SiO_2 layer in the gap region and contribute to the switching? From this starting point, the intrinsic resistive switching and memory effects in silicon oxide (SiO_x, x = 1~2) will be gradually revealed in the following chapters.

Chapter 2

Resistive Switching in Planar Nanogap Systems on SiO_x ($x \sim 2$) Substrates

— An Electrode-Independent Switching Scenario

2.1 Motivation and Outline

For the reasons discussed in Section **1.4**, it is important to carry out the study of local field effects on resistive switching in similar nanosystems, in particular, to clarify whether it is safe to attribute the switching only to the electrode materials without invoking the participation of the SiO_x (x~2) substrates. In this regard, various nanogap systems with different materials were made on SiO_x substrates to study the electrical property.

In this chapter, voltage-controlled resistive switching is demonstrated in various gap systems on SiO_x substrates. The nanosized gaps are made by several means using different materials including metals, semiconductors and amorphous carbon. The switching site is further reduced in size by using multi-walled carbon nanotubes and single-walled carbon nanotubes. The switching in all the gap systems shares the same characteristics. This independence of switching on the material compositions of the electrodes, accompanied by observable damage to the SiO_x substrate at the gap region, bespeaks the intrinsic switching from post-breakdown SiO_x. It calls for caution when studying resistive switching in nanosystems on oxide substrates, since oxide breakdown extrinsic to the nanosystem can mimic resistive switching. Meanwhile, the high ON/OFF ratio (~10^5), fast switching time (2 μs, tested limit), and durable cycles show promising memory properties. The observed intermediate states indicate the filamentary nature of the switching.

2.2 Resistive Switching in Various Nanogaps[52]

2.2-1 Lithography-Defined Metal-Metal Nanogap

Shown in Fig. 8a is a metal-metal nanogap system by a pair of tungsten (W) electrodes separated by ~50 nm on a thermal-oxidized Si surface (the SiO_x thickness is 200 nm, and the same thickness is used for all the following devices, unless otherwise specified), defined by a standard electron beam lithography (EBL) and lift-off process. Note that for EBL, positive resist polymethyl methacrylate (PMMA) was used. It was comparatively difficult to achieve line width below 100 nm (> 2 μm long). Short-time ultra-sonication was usually adopted to assist the lift-off process, so a titanium (Ti) adhesion layer (*e.g.*, 5 nm) between the W electrodes and the SiO_x substrate was necessary. For the nanogap systems discussed in this chapter, the electrical characterizations were performed using an Agilent 4155C semiconductor parameter analyzer and a data acquisition system (NI USB-6251 BNC) in a vacuum environment (~10^{-5} Torr).

Bias voltage was applied between the two electrodes by sweeping from 0 V to 30 V and then back to 0 V (Fig. 8b). The device shows no conduction during the initial forward sweep from 0 V to 25 V (*e.g.*, the current is at the noise level, ~10^{-12} A, of the instrument). Substantial conduction begins at ~25 V with a sudden current increase at ~30 V, indicating a SiO_x breakdown. An irreversible resistance change takes place in the post-breakdown device, indicated by the increased current level during the

subsequent backward sweep from 30 V to ~6 V. The sudden current (or conductance) rise at ~6 V (indicated by the red arrow in Fig. 8b) in this backward sweep indicates the initiation of hysteretic current-voltage curves (*IV*s) essential for memory switching. Fig. 8c shows the two characteristic *IV*s of the post-breakdown device: in a forward sweep (0 V → 10 V, blue curve), beginning with an OFF state, the device jumps to an ON state at ~3.5 V and goes back to OFF at ~5 V. In the backward sweep (10 V → 0 V, red curve), it jumps from an OFF state to an ON state at ~5 V and keeps the ON state below 5 V. (Note: A fast voltage drop edge[20] is expected at the end of each forward sweep, which sets the device state. So the beginning conduction state for a forward sweep is determined by the previous forward sweep. Here the characteristic forward *IV* was obtained after at least another forward sweep prior to it in the same voltage range. So it begins with an OFF state. All the following characteristic forward *IV*s were obtained in this way, unless otherwise specified.) Consequently, a current hysteresis is produced in the bias range below 3.5 V (region "**I**" in Fig. 8c). The underlying information about the two *IV*s is that a fast voltage drop edge above 3.5 V (region "**II**" in Fig. 8c) can set the conductance of the device into a value corresponding to the set voltage.[20] For example, a +4 V pulse "writes" the device into an ON state, while a +10 V pulse "erases" the device to an OFF state. The set states can be read out in the lower bias region **I** without being destroyed, demonstrating the non-destructive memory property. Fig. 8d shows the corresponding memory cycles in the device, with an ON/OFF ratio close to 10^5.

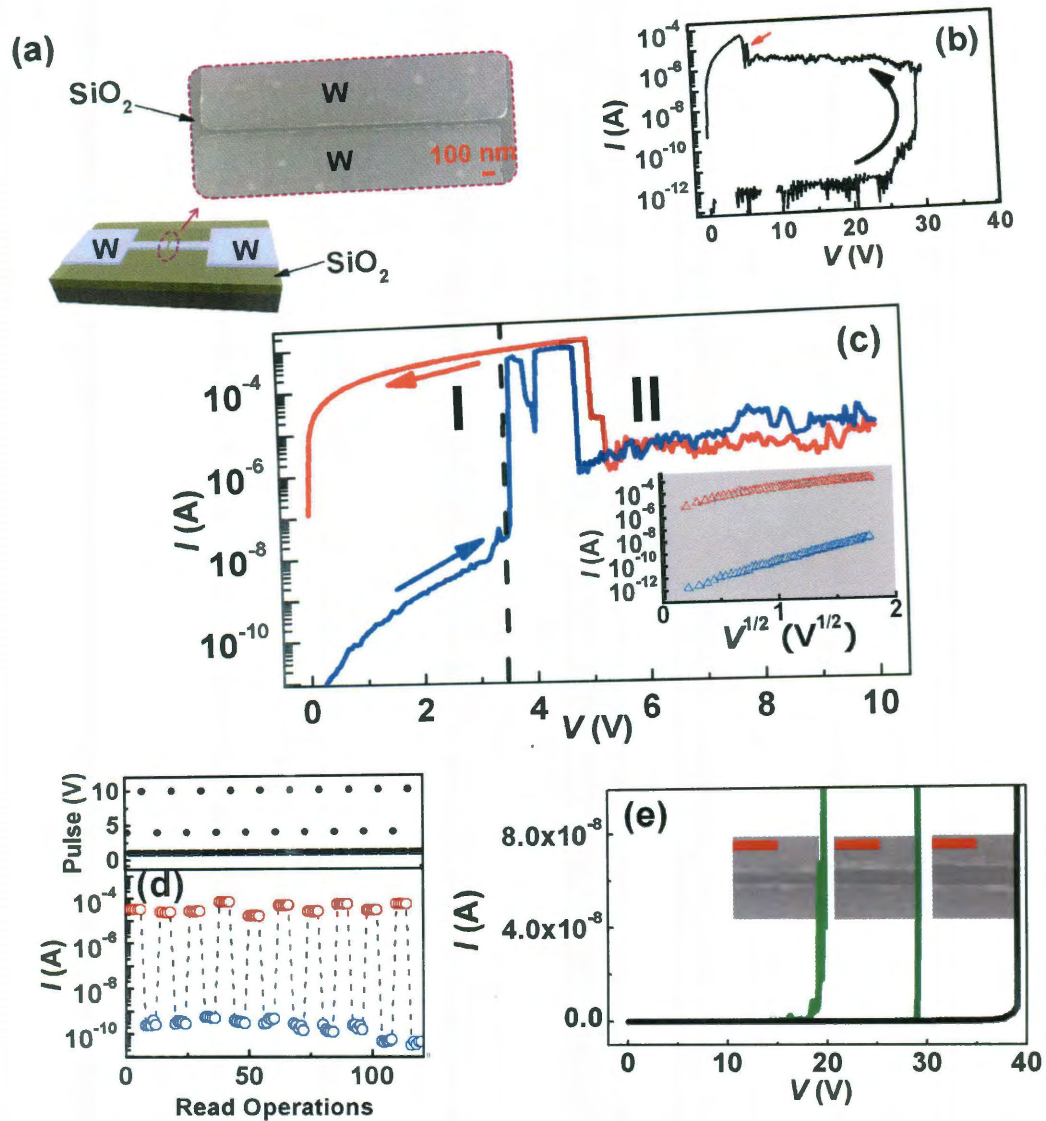


Figure 8. (a) Schematic of the W-W gap and the SEM image. (b) *IV* of the initial sweep from 0 V → 30 V → 0 V in the as-made 50nm-gap device. (c) *IV*s of a forward (0 V → 10 V, blue curve) and subsequent backward (10 V → 0 V, red curve) in the electroformed device. The black dashed vertical line separates region "**I**" (reading) and region "**II**" (writing/erasing). The inset shows the *IV*s in region "I" using an $IV^{1/2}$ plot. (d) Memory cycles of the device: after every five readings at +1 V, the device was set by an erasing pulse +10 V or a writing pulse +4 V. The top panel shows the corresponding pulses. (e) *IV*s in three as-made devices with W-W spacing of 30 nm (green curve), 50 nm (dark green curve), and 70 nm (black curve). The pictures beside each curve show the corresponding SEM images of the devices, with the red scale

bars 100 nm in length.

The SiO_x breakdown induced conduction is supported by the linear dependence of breakdown threshold voltage on the electrode-electrode spacing. Gap spacing of ~30, ~50, and ~70 nm result in breakdown threshold values of ~18 V, ~29 V, and ~39 V, respectively (Fig. 8e). The corresponding averaged electric field is ~6 MV/cm, which falls into the typical breakdown values of SiO_x.[51] The surface region is also expected to induce breakdown more easily than bulk given the higher likely density of defects. The sudden current increase during the first sweep is accompanied by observable SiO_x substrate damage in the gap region. Subsequent forward or backward sweeps usually undergo gradual current increases and fluctuations having the characteristics increasingly like those of the forward or backward *IV*s depicted in Fig. 8c. This electroforming process resembles that observed in vertical M/SiO/M ("M" denotes conducting electrodes) switching systems,[20] in which the amorphous form of SiO is the conducting and switching medium. The non-ohmic *IV*s, both for ON and OFF states, are dominated by Poole-Frenkel conduction having the characteristic of $\log(I) \propto V^{1/2}$ (inset in Fig. 8c). Using the Poole-Frenkel expression[53] $I = I_0 \exp(\frac{\beta_{PF} E^{1/2}}{kT})$ for fitting (k is the Boltzmann constant, T the temperature, and E the electric field; here T is at room temperature 300 K and the gap width d = 50 nm ($E=V/d$)), we obtain a Poole-Frenkel field-lowering coefficient ($\beta_{PF} = 3.4 \times 10^{-5} eVm^{1/2}V^{-1/2}$) from the OFF state is very close to the theoretical one

of $\beta_{PF} = 3.8\times10^{-5} eVm^{1/2}V^{-1/2}$ and other experimental values in SiO_x.[53]

2.2-2 Amorphous-Carbon Nanogap System

Contests could arise in the above representation of a pair of bare metal electrodes on SiO_x, as metal filament (conduction through metal migration from the two electrodes at high electric filed) can be implicated. One way to address this valid concern is to use nonmetal electrodes.

The electric field assisted breakdown in conducting materials[47,49,54,55] offers another means for nanogap generation in nonmetal films. A lift-off process was used to define an amorphous carbon (α-C) stripe (~ 40 nm thick, by sputtering from a carbon graphite target) on a SiO_x substrate. Two platinum (Pt) electrodes, with a comparatively large spacing (~0.8 μm), were then defined (see top inset in Fig. 9a). A 5-min annealing at 600 °C in Ar/H_2 environment (Ar and H_2 flow rates are 450 sccm and 150 sccm, respectively) was performed to improve the conductivities of both α-C layer and contacts. This annealing process, however, was not necessary if the sputtered α-C layer had comparatively good conductance (*e.g.*, ρ ~ several KΩ/□). Electrical annealing (*e.g.*, by several voltage sweeps up to 4 V) can be adopted in the vacuum environment to improve the electrical conductance, largely at the α-C/Pt contacts. Bias voltage was applied between the two electrodes. The sudden current drop at ~5.8 V (Fig. 9a) indicates a breakdown in the α-C stripe. A scanning electron microscope (SEM) image reveals a cracked region perpendicular to the current

direction in the α-C stripe (Fig. 9b). Note that the electrical breakdown voltage value is dependent on the Pt-Pt electrode spacing and the α-C material. Usually it is suggested that the Pt-Pt spacing is within several micrometers region in order to have successful electrical breakdown in the α-C layer within the equipment range (*e.g.* < 40 V). The reduced conduction immediately after the α-C breakdown (see the subsequent backward sweep in bottom inset in Fig. 9a) has similar Poole-Frenkel feature to that seen in Fig. 8c, indicating the disruption of the α-C layer and simultaneous breakdown in SiO_2 in the gap region. The conductance jump at ~6 V (bottom inset in Fig. 9a) during this backward sweep, initiates the similar electroforming process as discussed above in the W-W gap (Fig. 8b). The characteristic forward *IV* (Fig. 9c) and switching (Fig. 9d) show similar features to those in the W-W gap (Figure 8c, d) such as current levels, writing/erasing voltages, ON/OFF ratio, and switching times. While the threshold breakdown voltage in α-C tends to be proportional to the electrode-electrode spacing, the writing/erasing voltages for switching tend to be independent of it, consistent with the local switching nature within the gap region; since the collective resistance of the contacts and α-C layer is considerably smaller than that of the gap region, the bias voltage largely drops across the gap.

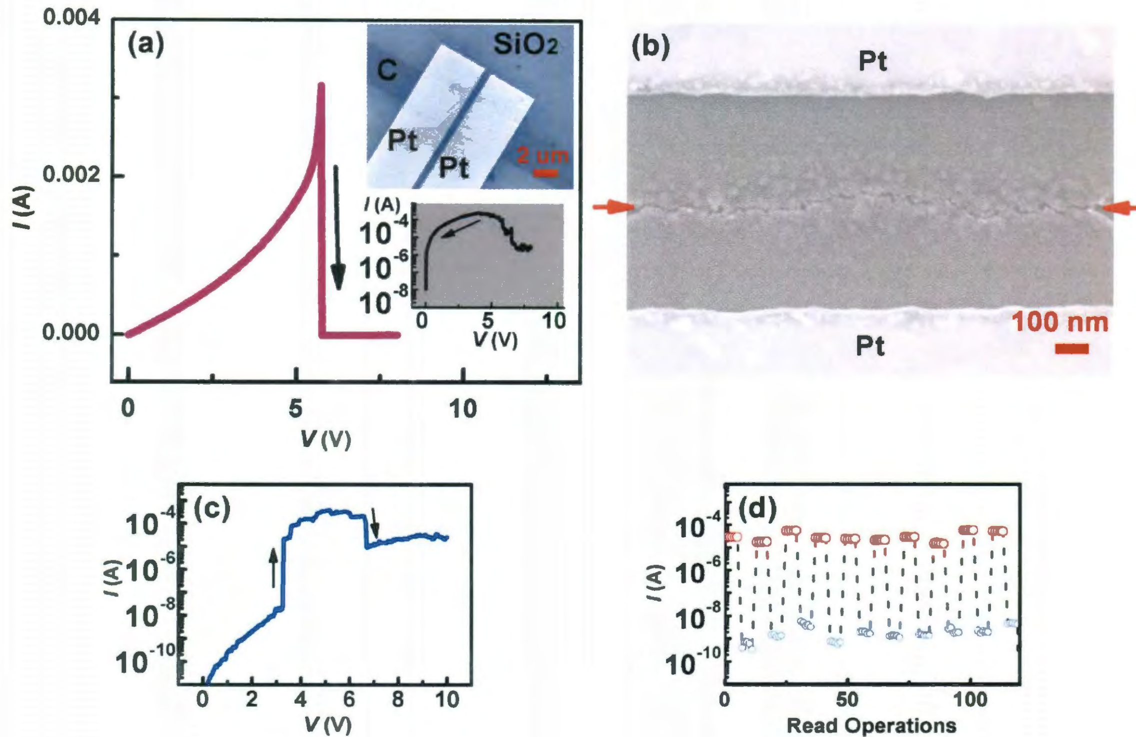


Figure 9. (a) *IV* of the initial forward sweep in the as-made α-C device. The top inset shows the SEM image of a patterned device. The bottom inset shows the *IV* of the subsequent backward sweep right after α-C breakdown. (b) SEM image of the α-C stripe between the two Pt electrodes after the α-C breakdown. The red arrows indicate the breakdown-induced gap region. (c) The characteristic forward *IV* in the electroformed device. (d) Memory cycles using +1 V (5 reads), +4 V (write), and +10 V (erase) pulses.

Compared to the EBL-defined W-W gaps, the α-C breakdown-induced gap reduces the initial breakdown and electroforming voltage of SiO_2 in the gap region since the narrowest part is expected to be smaller than 30 nm. Also, the production of these devices requires a less demanding fabrication process as no sub-100 nm line features are required. The switching behaviors are quite similar to those observed in

nanocable structures,[49] in which the outer graphitic shell was grown by CVD method and much more ordered in sp^2 forms. It was because of these ordered sheet structures that electromechanical motion between individual sheets at the gap region was proposed to be the switching cause.[49] A simple argument should follow that the configuration of microstructures of individual carbon sheet should affect the switching to a point. However, despite the difference in microstructure between CVD carbon and amorphous carbon, which has more sp^3 components and is more disordered, the switching behaviors are quite similar between the two systems.

The carbon form offers a better way to investigate the details of the gap region by removing the α-C layer without destruction to the SiO_x substrate. α-C was removed by oxidation (750 °C annealing in air) in the same switching device. SEM images show substantial damage to the SiO_x part corresponding to the gap region (compare Fig. 10 a and b). Further control tests were performed in devices with same α-C thicknesses and electrode spacing to investigate how the damage to SiO_x forms. In one group, we performed multiple sweeps up to a voltage slightly below the α-C breakdown threshold value (thus no gap generation, see Fig. 11a), while in the other we produced breakdown in the α-C layer by one single sweep to a voltage above the α-C breakdown threshold value (see Fig. 11b). After the α-C removal, observable damage to the SiO_x substrate at the gap region in the second group was found, but no damage to the SiO_x substrate was found in the first group. The results reveal that: 1) the gap generation in the α-C layer simultaneously induces SiO_x breakdown within

the gap region, which is consistent with the reduced conduction (through post-breakdown SiO_x) having the Poole-Frenkel feature right after the α-C breakdown discussed above; 2) the damage to SiO_x is mainly through local electric-field induced breakdown, as opposed to local heating, since a great reduction in current local heating is expected after the disruption of α-C layer in the gap region due to the sudden current drop. We also found that extended electroforming process and switching cycles tend to have more pronounced damage to SiO_x substrate in the gap region. These results indicate the role of SiO_x in switching in the gap region.

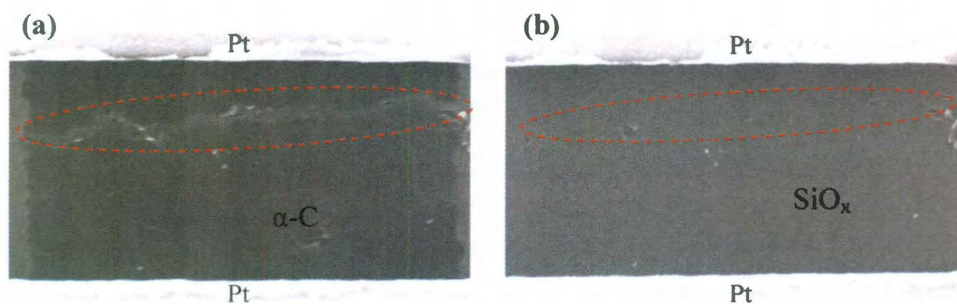


Figure 10. (a) SEM image of a switching α-carbon stripe, showing gap feature (circled by red dashed curve). (b) After carbon removal, damage to the SiO_x substrate at the gap region was found (circled by the red dashed curve).

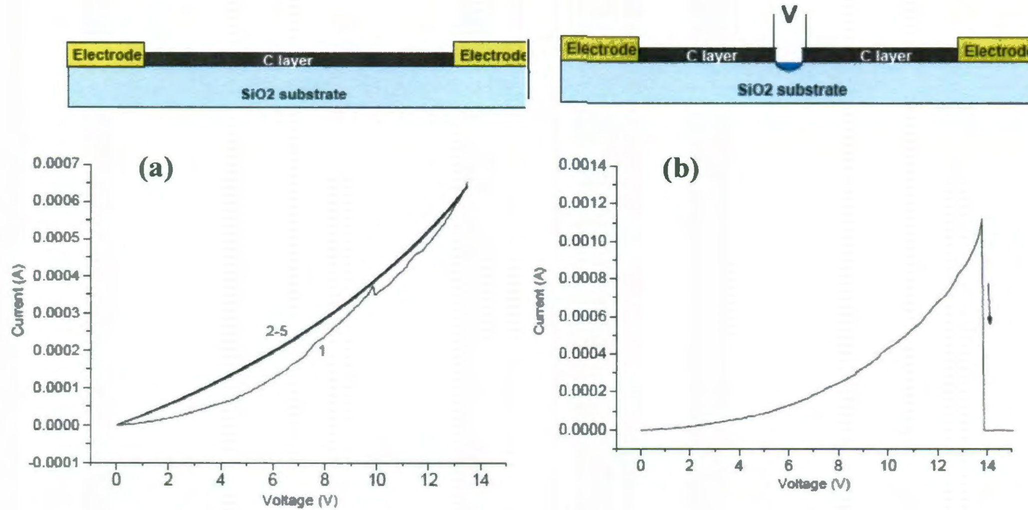


Figure 11. (a) Multiple *IV* sweeps (up to 13.5 V, which is slightly lower than the threshold breakdown value of 14 V) in a carbon stripe without initializing breakdown in the carbon layer. (b) A single sweep to 15 V induces the breakdown in the carbon layer.

2.2-3 Titanium Nitride Nanogap

The post-breakdown SiO_x switching nature is further emphasized by using a different material as the gap generation medium. Electrical breakdown in a titanium nitride (TiN) stripe on a SiO_x substrate leads to similar gap structure and switching (see Fig. 12). Compared to that in α-C stripe, the gap in a TiN stripe is usually located at the TiN-electrode interface instead of between the electrodes. The possible reason is that the Schottky barrier at the TiN-electrode interface (since TiN is semiconducting) enhances the local field and facilitates the TiN breakdown at that location, as opposed to an efficient C-Pt electrical contact in the α-C stripe, where breakdown in α-C is likely to happen at the least heat-dissipation region far away from both electrodes.

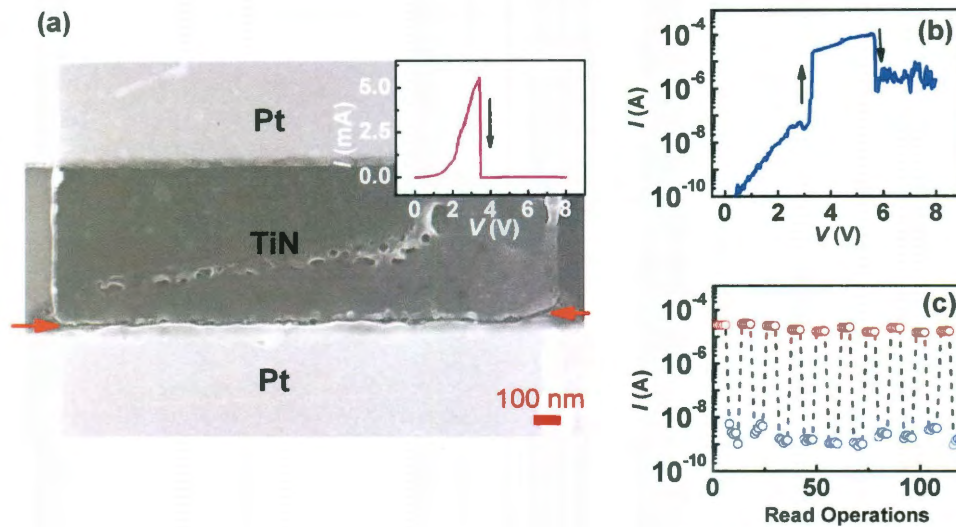


Figure 12. (a) SEM image of a switching TiN stripe on SiO_x substrate. The red arrows indicate the gap region induced by an initial TiN breakdown. The inset shows the initial TiN breakdown *IV*. (b) The characteristic forward *IV* in the electroformed TiN device. (c) Memory cycles using +1 V (5 reads), +4 V (write), and +7 V (erase) pulses.

2.2-4 Nanogaps Formed by Metal Islands

A gap due to electric field breakdown is less likely to form in metal stripes because the high current density usually melts the metal before a breakdown and the surface tension of liquid metal tends to form droplets, preventing a narrow and well aligned gap. However, a thin metal film tends to form discrete islands,[56] and nanogaps may form naturally between individual islands. For this purpose, an aluminum (Al) thin film (~10 nm thick) was deposited by sputtering on SiO_x between two Pt electrodes. The surface morphology of the deposited Al studied by atomic force

microscope (AFM) shows discontinuous granular features (Fig. 13a). A voltage sweep was applied between the two electrodes for the as-made device. Unlike that in α-C or TiN stripes, the initial forward sweep (0 V → 20 V) shows a much lower conductance and no sudden current drop (Fig. 13b). This further indicates the discontinuity of the Al film. The subsequent backward sweep (20 V → 0 V), with a conductance jump, indicates the initiation of hysteretic behavior. The SEM image of the electroformed device shows a granular Al surface between the electrodes (Fig. 13c) with no such apparent gap (Fig. 13d) as that produced by breakdown in α-C or TiN stripes, which is consistent with the *IV* feature of the initial sweep discussed and in support of the idea of switching in as-formed island-island gaps. Although the actual switching site is unknown due to numerous indistinguishable gaps between islands, it is expected that the relatively high resistance of the Al film reduces both the current and effective voltage drop across the switching site. Therefore, the switching device has higher writing/erasing voltages (Fig. 13e) and lower ON current (Fig. 13f). Following this idea, using other conducting metallic nanoparticles (*e.g.* self-assembled nanoparticles from bottom-up), although not yet demonstrated, could also do the same job to induce resistive switching on SiO_x substrate.

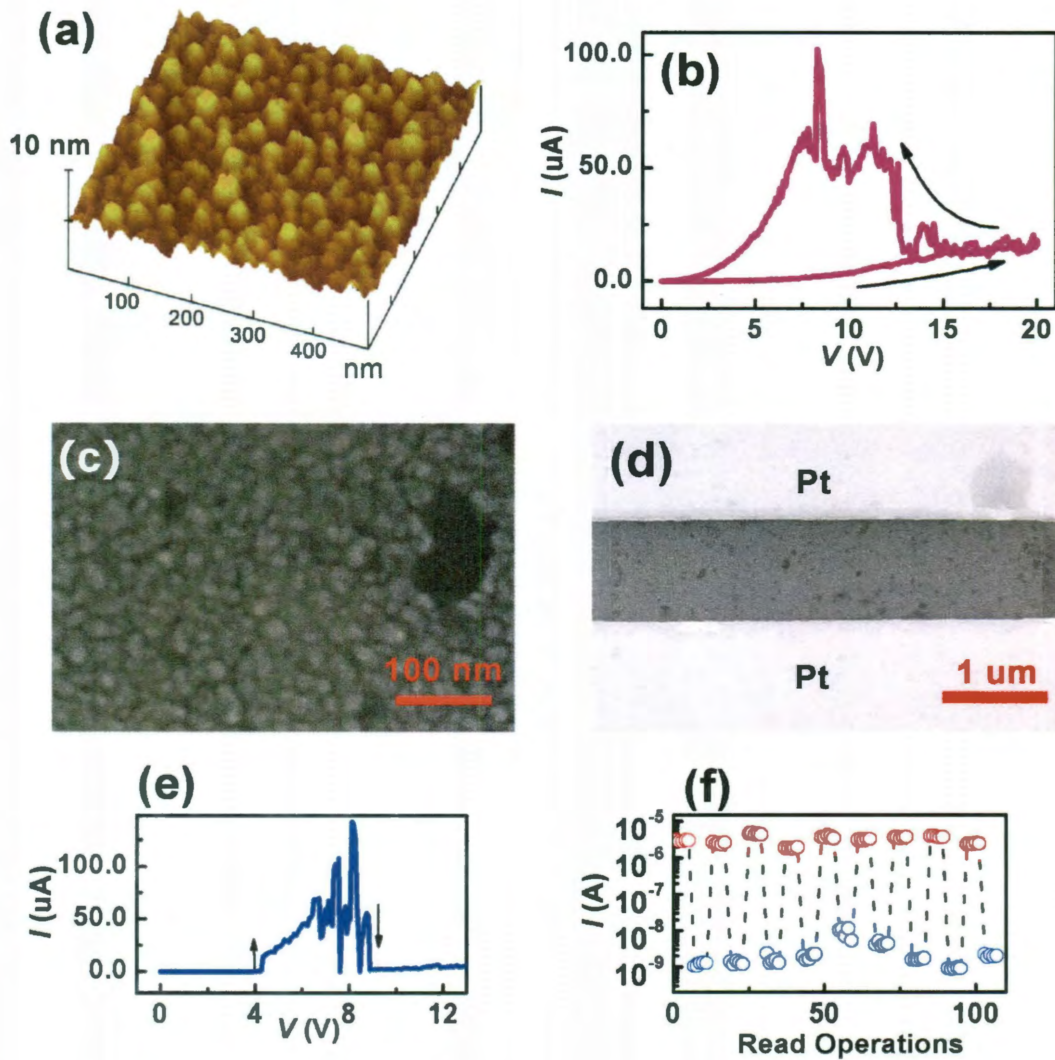
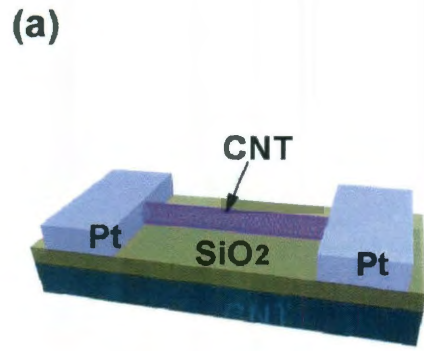


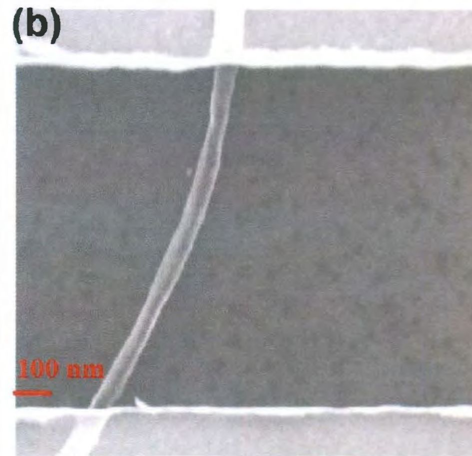
Figure 13. (a) AFM surface morphology of Al film between the two Pt electrodes. (b) *IV* of the initial double sweep (0 V → 20 V → 0 V, indicated by the black arrows) in the as-made Al-island device. (c) SEM image of the Al film of the switching device, showing the granular structures. (d) SEM image of the Al-island after switching, showing no apparent gap structure. (e) The characteristic *IV* of a forward sweep in the electroformed Al-island device. (f) Memory cycles using +1 V (5 reads), +6 V (write), and +14 V (erase) pulses.

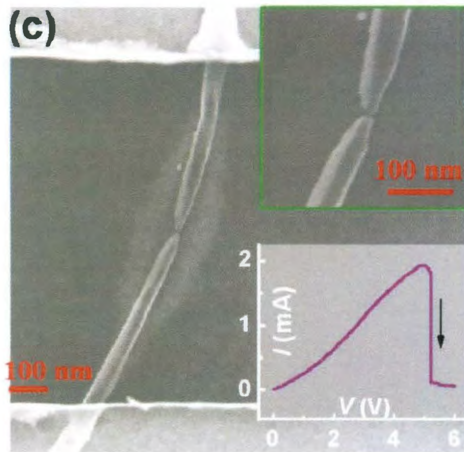
2.2-5 Nanogaps by Multi-Walled Carbon Nanotubes

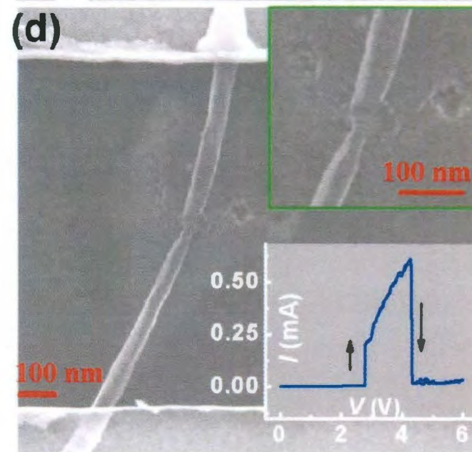
From the device perspective, one interesting question is, how small can the device become? Furthermore, a small and constricted switching size may offer a clearer view of the switching location, while it is relatively difficult to distinguish the actual switching site in a wide α-C stripe, *e.g.*, whether the switching happens uniformly along the entire gap region or locally. The electrical breakdown in MWCNTs[57,58] provides a potential means for further reduction in gap size. For this purpose, two Pt electrodes were patterned on the ends of a MWCNT[59] (Mitsui & Co., Ltd.) with a diameter ~60 nm (Fig. 14a). Fig. 14b shows the SEM image of the pristine device. Electrical breakdown begins at a voltage ~5 V indicated by a sudden current drop (bottom inset in Fig. 14c). The corresponding SEM image right after this breakdown shows a broken gap region (Fig. 14c and top inset). The subsequent sweeps electroform the device, showing the characteristic switching *IV* (bottom inset in Fig. 14d) similar to those observed in all the above devices. The SEM image of the electroformed device shows clear damage to the SiO_x at the gap region, extending beyond the nanotube (Fig. 14d and top inset). Note that switching in electrical breakdown MWCNTs was reported previously.[60] The ON and OFF states were achieved by close-and-break motion of the carbon nanotube shells from the two broken ends, and were stable up to only several cycles.[60] The switching here is attributed to the post-breakdown SiO_x at the gap region and is stable with extended cycling (Fig. 14e). The non-mechanical switching of the nanotube itself is also supported by the high yield in our devices (*e.g.* 10 out of 10 MWCNT devices tested show similar switching) regardless of the actual details of the broken ends (more

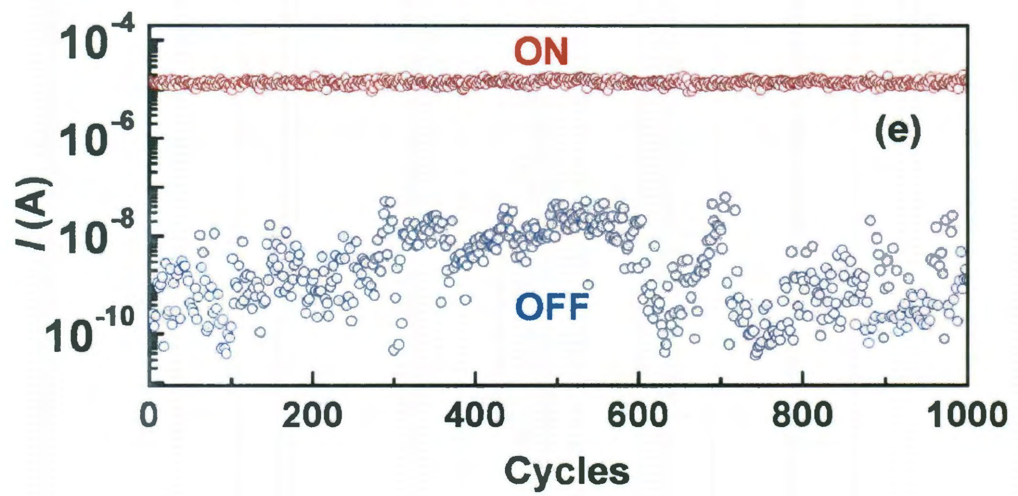
examples can be found in Fig. 14f-i). This is in contrast to nanotube-based mechanical switching since we expect that both the broken gap size and the morphology of the broken ends would affect the behavior. It should be noted that these broken nanotube ends maintained contact with the SiO_x substrate and the gap sizes were within 50 nm. Imaging did indicate extreme cases when the broken nanotube ends were curved upward and/or spaced far away from each other (> 100 nm).


(a)
CNT
Pt
SiO2
Pt


(b)
100 nm


(c)
100 nm
100 nm
I (mA)
V (V)


(d)
100 nm
100 nm
I (mA)
V (V)


ON
OFF
(e)
I (A)
Cycles

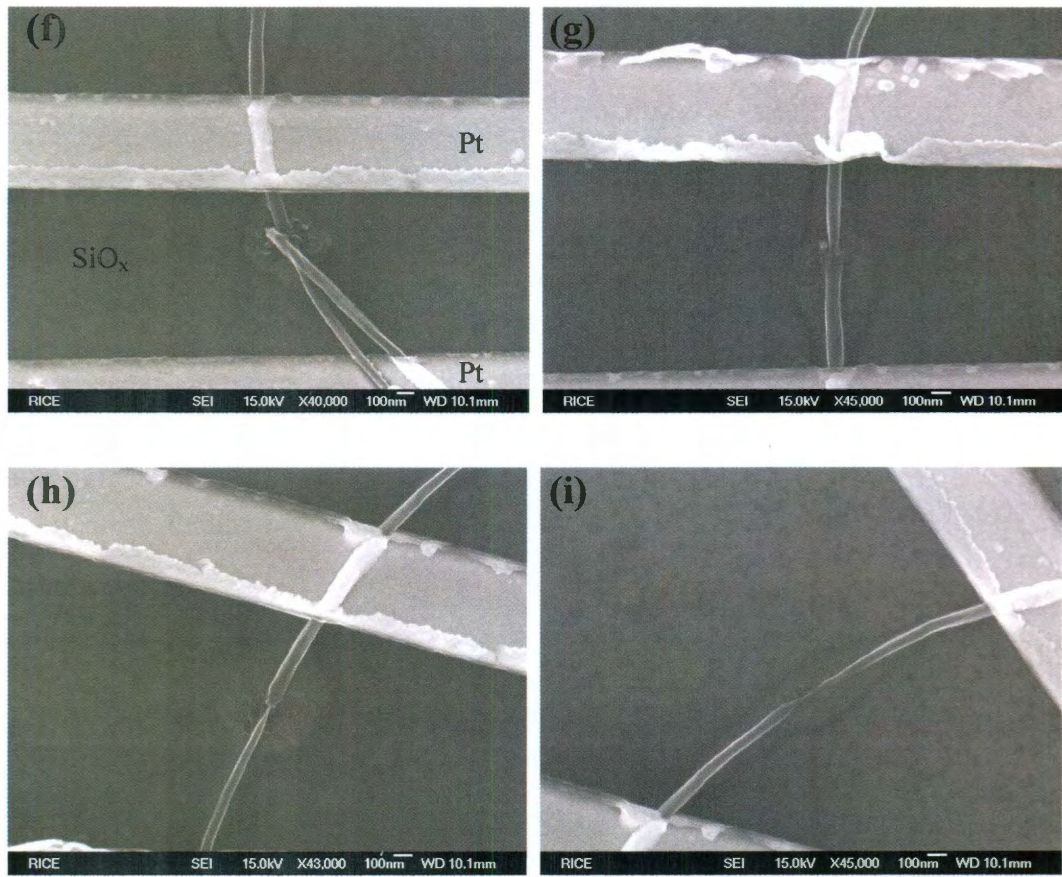
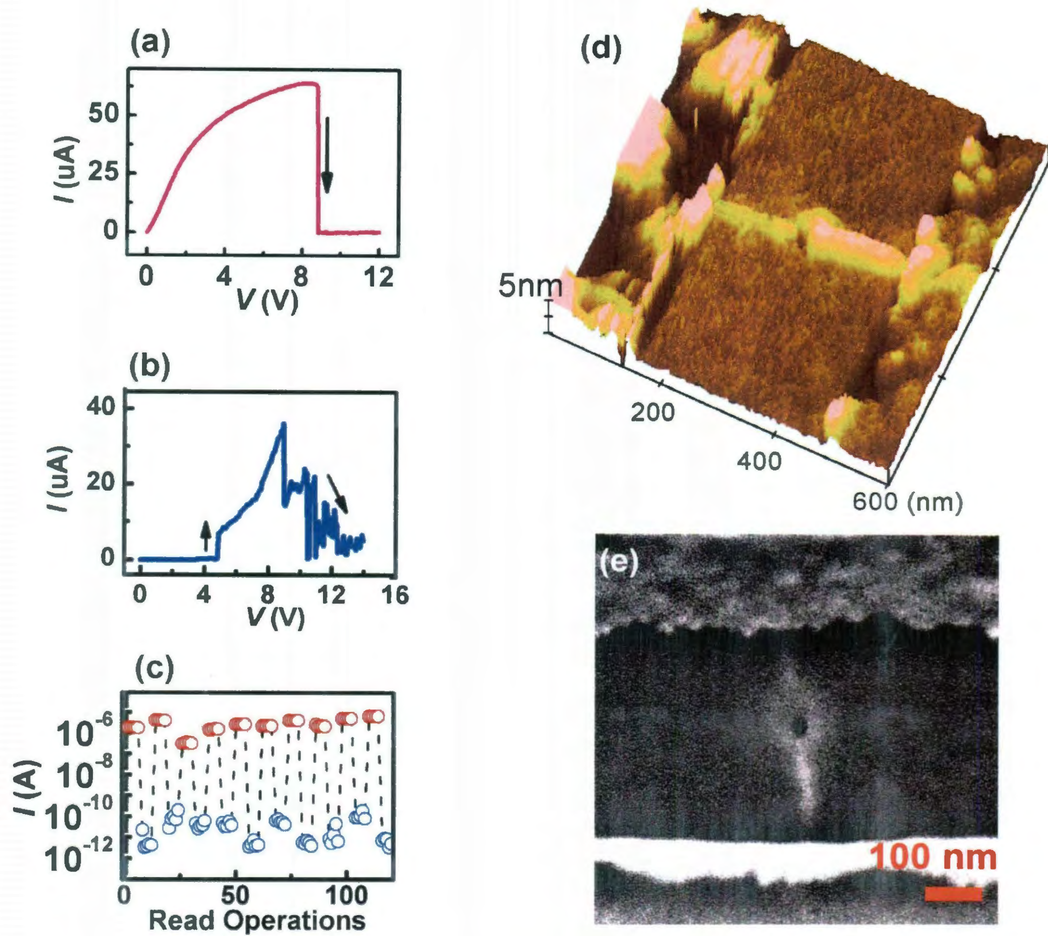


Figure 14. (a) Schematic of two Pt electrodes patterned on a MWCNT atop a SiO_x substrate. (b) SEM image of the as-made MWCNT device before electrical characterization. (c) SEM image of the same MWCNT immediately after breakdown. The bottom inset shows the breakdown *IV* and the top inset is a magnified view showing the gap structure at the breakdown region. (d) SEM image of the same MWCNT device after electroforming. The bottom inset shows the corresponding characteristic forward *IV* and the top inset is the magnified view of the gap region showing SiO_x damage. (e) 10^3 cycles in a second MWCNT device, with the reading, writing, and erasing pulses of +0.5 V, +3.5 V, and +6 V, respectively. More SEM images of switching CNT-SiO_x-CNT nanogap systems are shown in (f)-(i).

2.2-6 Nanogaps by Single-Walled Carbon Nanotubes

Single-walled carbon nanotubes (SWCNTs) are candidates for ultra-small constrictions. Electrical breakdown in metallic SWCNTs was reported and used as a means for sorting semiconducting SWCNTs.[61] Ti/Pt electrodes were patterned on a metallic SWCNT with a diameter ~2 nm. Electrical breakdown takes place at ~8.5 V (Fig. 15a). Fig. 15b, c show the characteristic *IV* and switching after breakdown and electroforming. The AFM image of the electroformed device shows the broken region in the SWCNT (Fig. 15d). The corresponding SEM image in Fig. 15e shows a dark dot at the gap region, indicating hole-like damage to the SiO_x substrate, which is also inferred from the AFM image. The comparatively small ON current (Fig. 15c) in the SWCNT device is mainly attributed to the contact resistance between the broken nanotube ends and the post-breakdown SiO_x in the gap region, as a good electric contact to metallic SWCNTs with diameters below 2 nm usually requires specific metals.[62] This contact resistance also reduces the effective voltage drop across the gap, resulting in higher writing/erasing voltages (Fig. 15b).


(a)
I (uA)
V (V)
(b)
I (uA)
V (V)
(c)
I (A)
Read Operations
(d)
5nm
200
400
600 (nm)
(e)
100 nm

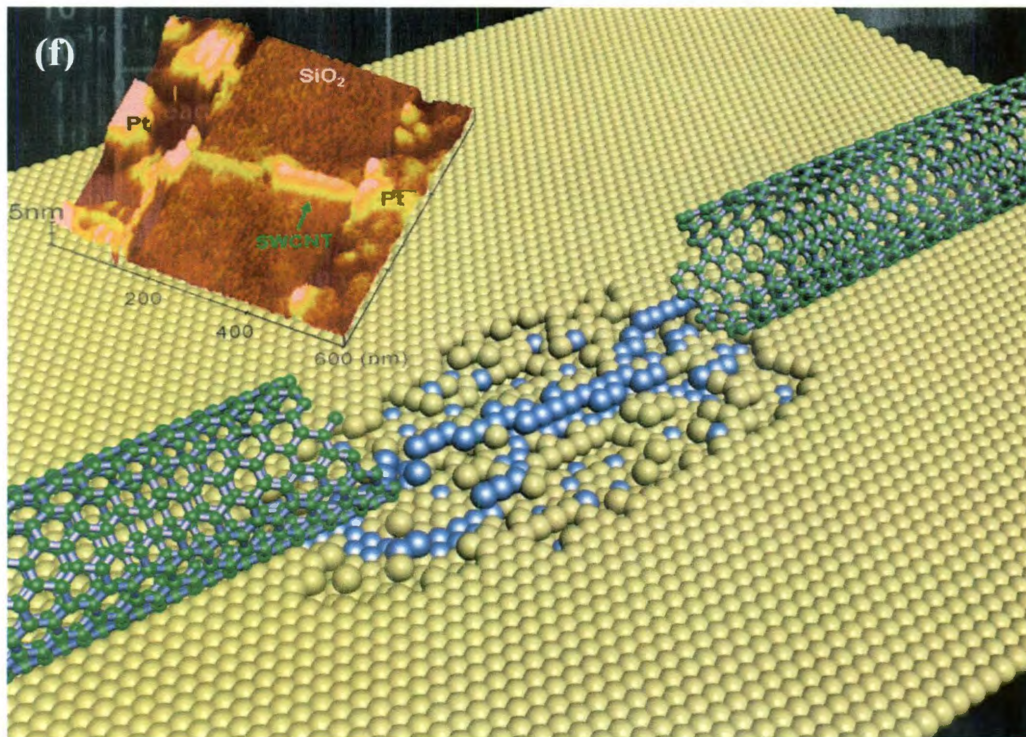

(f)
SiO2
Pt
Pt
5nm
SWCNT
200
400
600 (nm)

Figure 15. (a) The initial breakdown *IV* of the SWCNT device. (b) The characteristic forward *IV* in the electroformed device. (c) Memory cycles using +2 V (5 reads), +8 V (write), and +14 V (erase) pulses. (d) AFM image of the electroformed SWCNT device. (e) Corresponding SEM image of the same electroformed SWCNT device. (f) A cartoon illustration of the SWCNT-SiO_x switching system.

2.3 Mechanism Discussions

In this SWCNT switching case, the argument for electromechanical mechanism weakens (Fig. 15f): with a diameter of ~ 2 nm for the SWCNT, how could the two broken ends stretch and retract reliably and repeatedly across a gap over 10 nm to form ON and OFF states? As a matter of fact, the above nanogap devices share the similarities once operational, regardless of the (effective) electrode compositions. These include similar writing/erasing voltages and currents (the reduced ON currents and increased writing/erasing voltages in Al-island and SWCNT devices are due to high film or contact resistances), switching times, and noise distributions. The comparatively large current fluctuation in the erasing bias region observed in all the devices is another characteristic of SiO_x conduction.[20] The approximate independence of switching on the (effective) electrode materials ranging from metals (W, Al), conducting nonmetal (C), semiconductor (TiN), to carbon nanotubes, along with the electroforming processes and observable damage to the SiO_2 substrate in the gap regions, bespeaks the intrinsic post-breakdown SiO_2 switching nature. This is confirmed by making similar α-C stripe structures on Si_3N_4 substrates, in which

switching was not observed after the gap generation (totally 30 α-C stripe devices were tested on Si_3N_4, with none formed similar reliable switching). Severe substrate damages were usually observed in the gap region following an attempt of electroforming (Fig. 16).

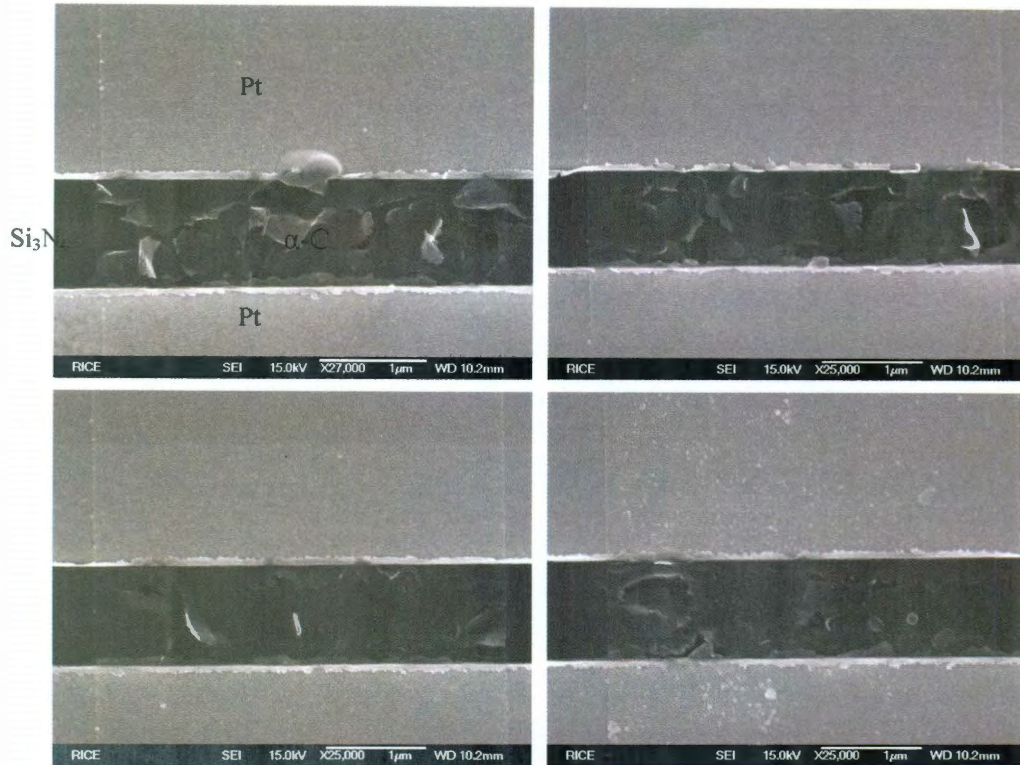


Figure 16. SEM images of α-C stripe devices on Si_3N_4 substrates followed by electroforming attempts. Severe damage to the Si_3N_4 substrates were always observed with no similar reliable switching observed.

Common features observed in all the above devices are the various intermediate conduction states. As shown in Fig. 17a, for an initially established MWCNT-based device, characteristic forward ($0 \rightarrow 7$ V) *IV* (green curve), an OFF state with a current

level of ~10^{-6} A can be set by a +7 V pulse (see cycles in the left column in Fig. 17b). By sweeping to a higher voltage above 7 V (black crossed curve), a lower conduction state appears, indicated by a sudden current drop at ~7.5 V (see black arrow). In the subsequent sweep, a new *IV* featuring a lower OFF state is established (see blue curve), and the same +7 V pulse now sets the OFF state to a current level of ~10^{-8} A (see cycles in the middle column in Fig. 17b). The OFF current can be further reduced by sweeping to an even higher voltage (see magenta crossed curve) during which a second conduction reduction appears at ~12 V (magenta arrow). This leads to a third *IV* (cyan curve) with an OFF current level of ~10^{-10} A that can be set by the same erasing pulse of +7 V (see cycles in the right column in Fig. 17b). Multiple intermediate conduction states are an indication of filamentary conduction in oxides,[63] in which different states can be viewed as formation/termination of new/existing percolation paths.[63,64] To an extent, the current fluctuations in the erasing region (see cyan curve in Fig. 17a) can be viewed as various meta-stable states, *e.g.*, same erasing voltages can produce different OFF currents if they encounter current fluctuations of different magnitudes. This is well-reflected in the 10^3 cycles of the MWCNT device, in which the OFF states undergo various conductance states (Fig. 14e). We attribute this to be the main cause of instability in the current device performance.

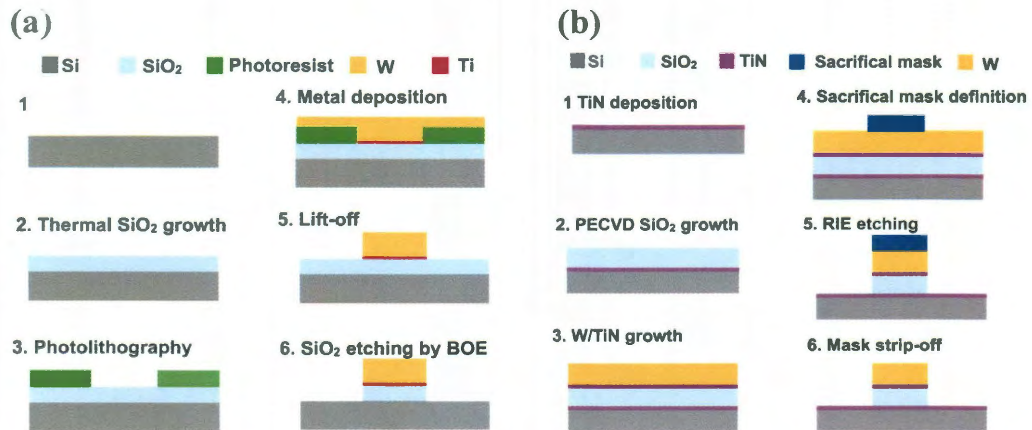
3.2 Resistive Switching in Vertical SiO_x with Metal Electrodes

3.2-1 Fabrication

Vertical sandwiched SiO_x structures with two different oxide growth methods were examined. In the first type of structure (Fig. 19a), SiO_x ($x \sim 2$) with a thickness of 50 nm was grown by thermal oxidation of a silicon substrate (the SiO_x/Si wafer was purchased from Silicon Quest International, Inc.). Then circular tungsten (W) electrodes (5 nm Ti was used as adhesion layer) with a diameter of 50 μm and thicknesses of 100 nm were defined by photolithography, metal sputtering, and a lift-off process. Buffered oxide etch (BOE, 10:1, J. T. Baker) was then used to remove the surrounding SiO_x, leaving the layer underneath the W electrode protected. Therefore, the W layer served as both a protective mask during etching and the top electrode for subsequent electrical characterization. It should be noted that the Ti adhesion layer is important in keeping the W layer adhered to the SiO_x substrate during the BOE etching. In general, the quality of the metal film also affects the quality of the SiO_x protection underneath. For example, chromium (Cr) is another metal often used as adhesion layer and its solubility in HF is low. A thick layer of Cr, ~ 100 nm, deposited using the same sputtering method; however, did not protect the SiO_x layer underneath, resulting in many pinholes in the SiO_x layer (Fig. 20). Those pinholes are most likely the cause of the immediate short circuit in devices or short circuits during the electrical testing. Likewise, a W/Cr combination with Cr as the adhesion layer does not well serve a protective role. In the second type of structure

(Fig. 19b), SiO_x with a thickness of 50 nm was grown by plasma-enhanced chemical vapor deposition (PECVD) on a TiN/Si substrate; TiN was deposited by physical vapor deposition (PVD) on Si. 10 nm of TiN and 100 nm of W were then deposited on SiO_x by PVD. A 70×70 μm^2 photoresist area was then patterned by photolithography and used as the sacrificial mask. Reactive ion etching (RIE) was used to define the vertical sandwich structures. Corresponding etching recipes (*e.g.*, $SF_6/BCl_3/Cl_2$ for W etching; BCl_3/Cl_2 for TiN etching; and CF_4/CHF_3 for SiO_x etching; the fabrication and etching processes were done by Sandisk Inc.) were used with the layered structure underneath the photoresist protected, thereby forming the vertical structure.

A several-minute annealing at 600 °C in an Ar/H_2 environment was performed before electrical characterizations. Measurements were done using an Agilent 4155C semiconductor parameter analyzer under a single sweep mode. Bias voltage was applied by a probe tip on the top W electrode with the conducting substrate grounded. All data was collected in vacuum (~10^{-5} Torr) at room temperature, unless otherwise specified.



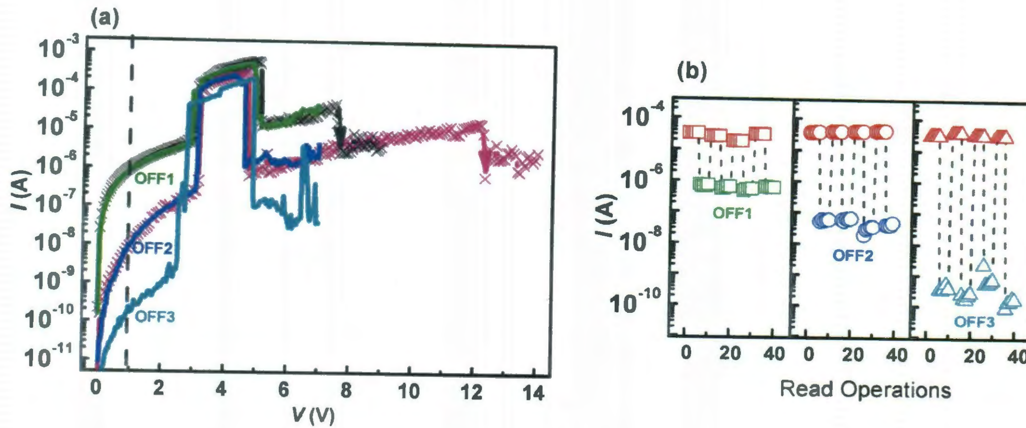


Figure 17. (a) *IV* evolutions in an electroformed MWCNT device. Starting from an initially established forward *IV* (0 V → 7 V, green curve), the subsequent forward sweep (black crossed curve) up to a higher voltage (0 V → 9 V) lowers the OFF state (see black arrow at ~7.5 V). A new characteristic forward *IV* with a lower OFF state is established subsequently (blue curve). By sweeping to an even higher voltage (magenta crossed curve), a second conductance reduction in the OFF state is initiated (see magenta arrow at ~12 V). Similarly, a third characteristic *IV* featuring even a lower OFF state establishes thereafter (cyan curve). (b) Memory cycles using the same set of +1 V (5 reads), +3.5 V (write), and +7 V (erase) pulses in the same device, with the left, middle and right columns corresponding to the established green, blue, and cyan characteristic *IV* curves in (a).

2.4 Summary

In this chapter, reproducible resistive switching in various nanogap systems on SiO_x substrates is demonstrated. The lack of dependence of the switching behaviors on electrode materials points to a common mechanism, post-breakdown SiO_x switching in the gap region. It is therefore important to exercise caution when building resistive switching nanosystems on SiO_x substrate. Effects should be taken to

Figure 19. (a) Fabrication process for vertical devices of type 1. (b) Fabrication process for vertical devices of type 2.

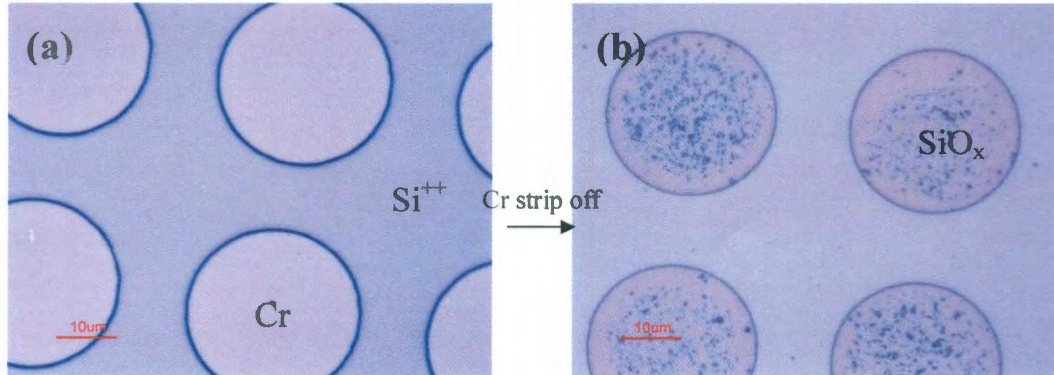


Figure 20. (a) In Cr-masked Cr-SiO_x-Si^{++} devices, after BOE etching and before Cr stripping, it appeared that Cr protected SiO_x underneath. (b) However, after the Cr top layer was stripped away, many small holes appeared in the SiO_x layer.

3.2-2 Characteristic *IV* Curves and Memory Switching

Fig. 21a shows the typical *IV*s in a first type of vertical W/Ti/(Thermal) SiO_x/Si device (DEV-1) by BOE (wet) etching under a forward (0→8 V) sweep and then a backward (8→0 V) sweep of the top electrode relative to the bottom one. The forward sweep features a high-impedance state at the low voltage region (denoted as region "**I**" divided by the vertical dashed line in Fig. 21a), with a sudden current jump at ~3.3 V and then a sudden drop at ~5 V into a high-impedance state again. The backward sweep, from high bias back toward 0 V, undergoes a low-impedance state at region "**I**". The underlying cause for this hysteretic behavior is a voltage-controlled permanent resistance change in the higher bias (writing) range (denoted as region "**II**" in Fig.

21a), indicated by the beginning of a sudden rise in current or conductance during the forward sweep. A rapid falling edge of voltage in this region can write the device into a conductance state corresponding to this ending voltage.[20] For example, a rapid voltage drop at 4 V writes the device into an ON state, while that at 8 V erases the device into OFF (In Fig. 21a, the forward sweep was obtained after at least one forward sweep performed to the same bias range; the device had been in an OFF state since a very rapid voltage drop to 0 V, at the end of the previous forward sweep, is expected to place the device into the corresponding high-impedance state). The obtained state can be read out at the low bias region "I" without being destroyed, rendering a non-volatile memory device. Fig. 21b shows a series of memory cycling in the device (Fig. 21b), with an ON/OFF ratio over 10^4 achieved. The *IV*s and switching behaviors obtained here are quite consistent and similar to that observed in the previous planar nanogap systems discussed in Chapter 2.

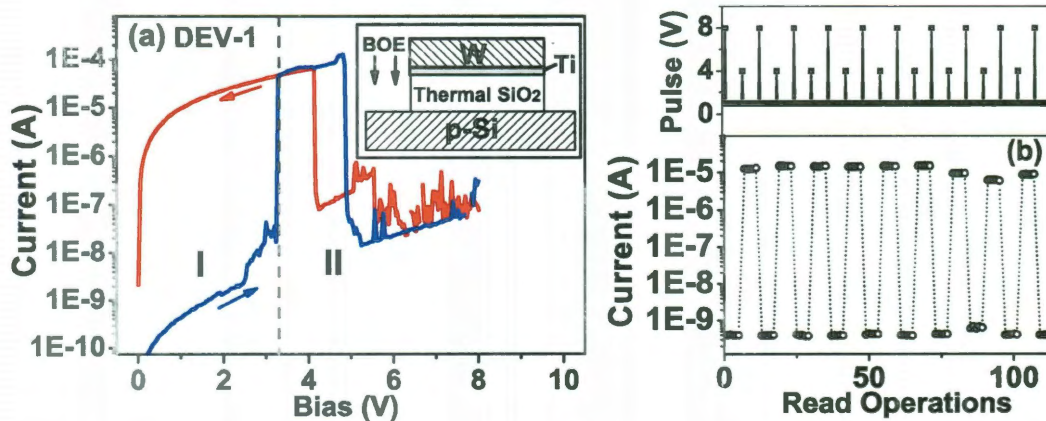


Figure 21. (a) *IV* curves of a forward (0→8 V) and subsequent backward (8→0 V) sweeps in DEV-1. The inset is a schematic of the device. The dashed line divides the bias regions of "I" and "II". (b) A series of reading the device state by applying bias

pulses of +1 V. After every five readings, the device was set by an erasing pulse (+8 V) or a writing pulse (+4 V) as show in the corresponding upper panel.

For the second type of structures of W/TiN/(PECVD) SiO_x/TiN/Si (DEV-2) were fabricated by RIE etching, a typical hysteresis *IV*s by similar consecutive forward and backward sweeps is shown in Fig. 22a. Compared to those in Fig. 21a from the wet-etching device, the *IV*s here have (1) higher ON and OFF currents and (2) comparatively smooth current changes in the writing region. The current or conductance change in this region, without a drastic rise or drop, means that the conductance state of the device can be changed semi-continuously by applying bias pulses of different amplitudes. The color curves in Fig. 22a show how different bias sweep ranges (thus different writing voltage at the end of each forward sweep) change the conduction states of the device (again, each set of forward and backward sweeps was obtained after at least one forward sweep preformed to the same bias range). With the decreasing of the sweep range, it shows a gradual decline in the ON/OFF ratio because of an increasing current in the OFF state set by the reduced ending bias (the ON current tends to increase at a rate much smaller than that of increase in the OFF current). The writing region tends to shift toward the low bias end, indicated by the shift of the current-rise edge in the forward sweep. A multilevel or analog memory[66] is demonstrated in Fig. 22b by applying erasing bias pulses of different amplitudes. The adjustable ON/OFF ratio is limited to up to 10^3 due to comparatively large OFF currents.

distinguish the switching cause. The high ON/OFF ratio, fast switching time, and durable cycles demonstrated here show interesting memory properties. In particular, the small switching site demonstrated in a SWCNT shows the feasibility of high-density SiO_x-based memory arrays if a vertical embodiment could be realized. The observed intermediate states reveal the filamentary conduction nature in post-breakdown SiO_x switching which is likely Si-Si wire formation, although a further investigation of the individual filamentary path is needed. The post-breakdown SiO_x conduction suggests another possible mechanistic scenario for the switching that was observed in graphitic memory.[49,65]

Chapter 3

Resistive Switching in SiO_x in Vertical Representations

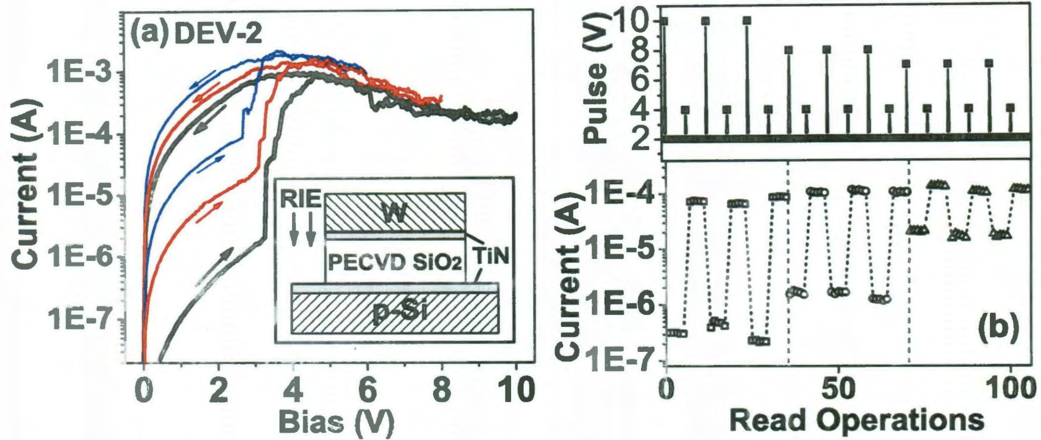


Figure 22. (a) A set of *IV* curves by forward and subsequent backward sweeps in DEV-2, with black (bottom), red (middle), and blue (top) curves corresponding to sweep bias ranges of 0-10, 0-8, and 0-6 V, respectively. Inset is a device schematic. (b) A series of reading the device state by applying bias pulses of +2 V (five reads between each set of writing-erasing pulses). The device undergoes OFF-state changes by applying applying erasing pulses of different magnitudes of +10 V, +8 V, and +7 V (with the writing pulse +4 V unchanged) as shown correspondingly in the upper panel.

3.2-3 Electroforming and Its Implication

In order to activate the pristine M/SiO_x/M into the resistive switching state described as in Fig. 21 and Fig. 22, some initial electrical stress (voltage), usually larger than the working voltages, needs to be applied to the device. This is also referred to as an electroforming process.[20] This process usually involves voltage sweeps to a certain value, upon which the conductance suddenly rises, accompanied with substantial fluctuations in the current. It should be also noted that, this current

3.1 From a Planar Structure to a Vertical

From a memory perspective, a vertical crossbar structure is needed for high-density data storage. Topologically, the planar nanogap switching systems discussed in Chapter **2** can be transferred into a vertical representation as illustrated in Fig. 18. Furthermore, if the SiO_x layer is thin enough, close to the width of the nanogap in the planar systems, no conducting film is needed to define the nanogap because the electrode-SiO_x-electrode structure itself already defines a gap having the width of the thickness of the SiO_x layer (Fig. 18c).

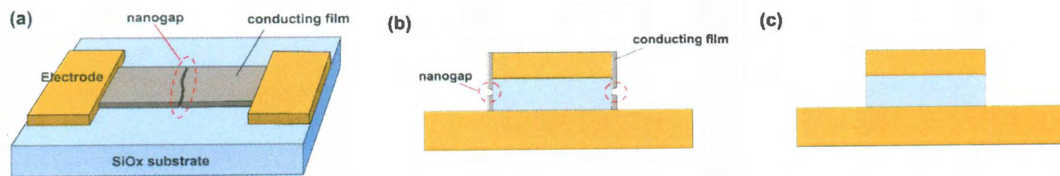


Figure 18. (a) An illustration for planar nanogap systems. (b) A vertical nanogap system with a conducting thin film at the vertical edges. (c) A vertical sandwiched structure of electrode-SiO_x-electrode without any conducting film.

In this chapter, the resistive switching phenomena and properties in vertical sandwiched E/SiO_x/E (here E denotes electrode) representation are demonstrated and discussed. From M/SiO_x/E (M denotes metal electrode) structures to metal-free E/SiO_x/E structures, very similar electrical behaviors are shown with the intrinsic SiO_x switching picture reinforced.

should at least increase to a level of several hundred nA (10^{-7} A). Then during the subsequent voltage sweeps, the voltage sweep range is gradually reduced while still keeping the current fluctuations, until at last the characteristic *IV* curve forms (Fig. 23). This electroforming process shares the same features as those observed in planar nanogap structures. For example, in an α-C stripe device on SiO_x substrate (Section **2.2-2**), the initial electrical breakdown in the α-C layer may produce a nanogap with a comparatively large size such that soft breakdown is not simultaneously induced in the SiO_x layer in the nanogap region. The α-C stripe device can still be activated into a switching state by a similar electroforming process (Fig. 24).

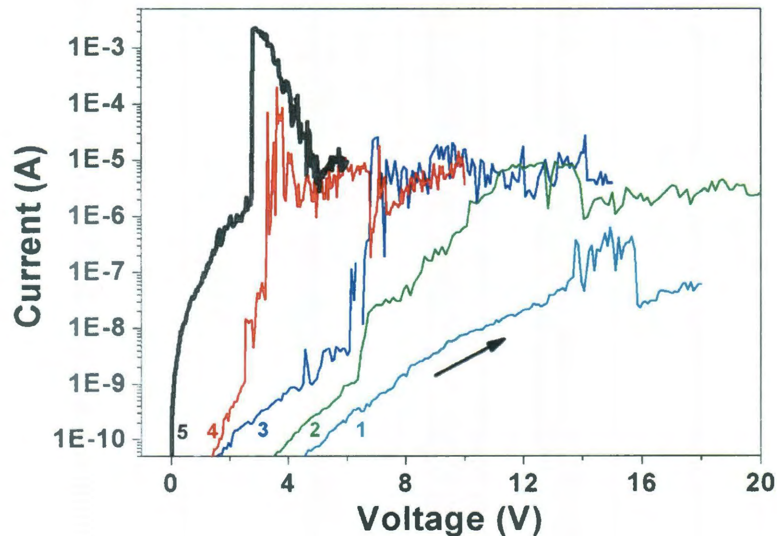


Figure 23. The Electroforming process in a $W/Ti/SiO_x/Si^{++}$ device after 5 min annealing in reducing environment at 600 °C. The black arrow indicates the voltage-sweep direction, and the numbers indicate the voltage-sweep orders.

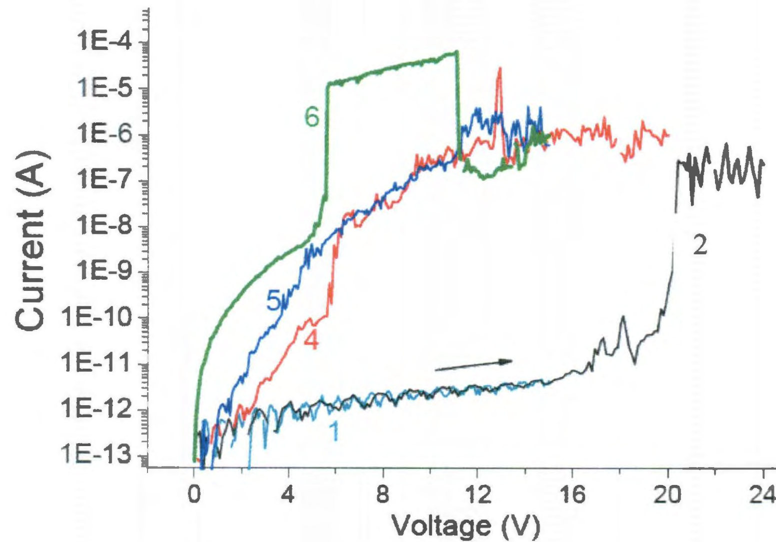


Figure 24. The Electroforming process in an α-C stripe device after the nanogap is generated by electrical breakdown in the α-C layer. The black arrow indicates the voltage-sweep direction, and the numbers indicate the voltage-sweep orders.

The electroforming site directly correlates to the switching site. To clarify where the switching takes place in these vertical devices, W or W/TiN electrodes with the same thicknesses and sizes were deposited on the (PECVD) SiO_x/TiN/Si substrate, without doing any etching of the oxide (see left schematic in Fig. 25a), or on wet-etching defined SiO_x pillars of larger diameter on the (thermal) SiO_x/Si substrate (see right schematic in Fig. 25a). The samples were then annealed under the same conditions as those adopted for the previous structures and then characterized via electrical measurements. No conduction was observed up to a bias of 25 V ($I \sim 10^{-12}$ A). Devices with different diameters (25 μm, 50 μm, and 100 μm) were also made and the ON currents were collected for DEVs-1 and another type of wet-etching

defined W/Ti/(PECVD) SiO2/TiN/Si devices (DEVs-3, see schematic in Fig. 25b). Statistically, for both DEVs-1 and DEVs-3, the ON currents follow a trend more closely to scaling with the diameter (black dashed lines in Fig. 25d-e) than scaling with the device area (red dotted lines in Fig. 25d-e). These results reveal that the conduction (thus switching) only takes place after the etching and is localized at the vertical SiO_x edges. On the other hand, the *IV*s of DEVs-3 tend to have some combined features of those in DEV-1 and DEV-2. For example, they typically have higher ON and OFF currents than those in DEV-1, but lower than those in DEV-2 (at the same bias sweep ranges). The forward sweep typically also begins with a sudden current rise in the writing region, but then follows a less intense declining tail. Fig. 25c shows three forward *IV*s from each of the three types of devices. These differences further indicate the role of the etched oxide edges in determining device behaviors. We expect surface differences not only resulting from different etching methods, but also from the same etching methods on SiO_x prepared by different growth techniques. One indicator of structural differences between oxides grown by varying methods is the difference in wet etching rates of PECVD SiO_x and thermal SiO_x.

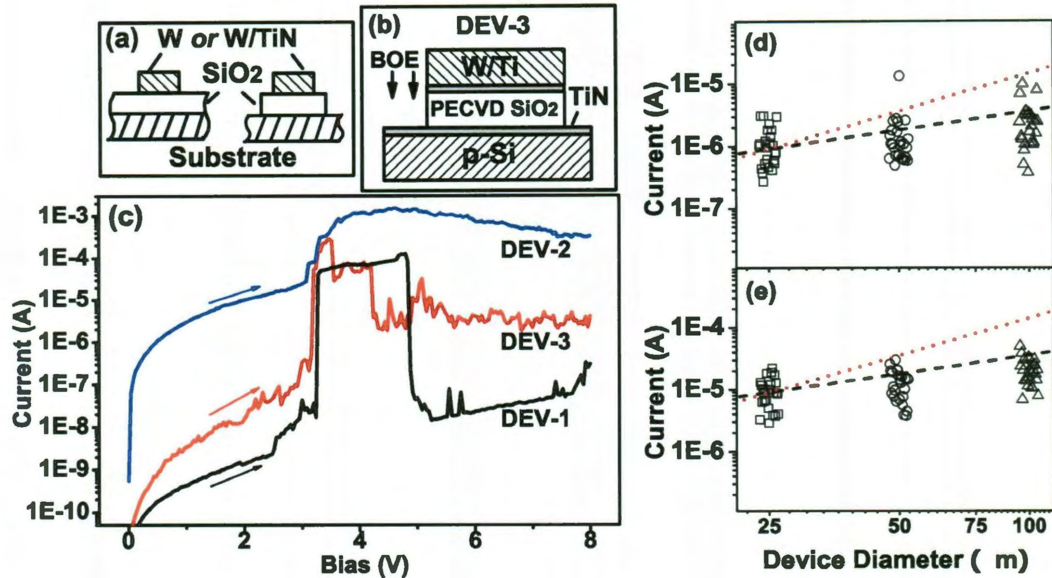


Figure 25. (a) Schematics of devices with (left) no SiO_x etching and (right) etched SiO_x pillar with a smaller on-top electrode. (b) Schematic of DEV-3. (c) A set of forward sweeps starting with the OFF states in the formed vertical structures of DEV-1 (black curve), DEV-2 (blue curve), and DEV-3 (red curve). (d) ON currents at +1 V (written by +5V pulses) for DEVs-1 and (e) ON currents at +1 V (written by +4 V pulses) for DEVs-3, with each type having device diameters of 25 μm (rectangles), 50 μm (circles), and 100 μm (triangles). 25 data points/devices were collected for each size. The dashed black lines describe a $I \propto D$ (diameter) scaling and the dotted red lines $I \propto D^2$ scaling.

The surface nature of the switching and conduction mechanisms in these vertical structures is further emphasized by the response of devices to annealing in a reducing atmosphere. A several-minute thermal annealing at 600 °C in Ar/H_2 was necessary to observe the switching in vertical devices produced by wet etching. Before annealing, a majority (over 80%) of the devices was non-conducting (*e.g.*, $I \sim 10^{-12}$ A at a bias up

to 25V). Detectable conduction began to take place after the thermal annealing in the reducing environment. By sweeping to a high voltage (*e.g.*, 20 V) within which some sudden current drops and large current fluctuations appeared, an electroforming process followed (see example as shown in Fig. 23). The current drops and fluctuations gradually moved toward lower bias voltages in the following sweeps, along with substantial increases in the current. Finally, reproducible forward *IV*s as described before were established. For the devices fabricated by dry etching (DEV-2), a similar forming process can take place even before the annealing. Thermal annealing could further increase the initial conduction and ease the electroforming process. All these features indicate the surface-related conduction.

Except for the aforementioned differences, these devices are similar in several aspects once operational. For example, they have (1) similar reading/writing bias ranges (Fig. 25c), (2) similar noise distributions with comparatively smooth *IV*s at the reading bias range and larger fluctuations in the writing region, and (3) fast switching time down to ~2 μs (test limit). Low-temperature tests show that these devices cannot be electroformed at a temperature below 150 K, while the ON-state conductance shows relatively little temperature dependence down to 100 K (Fig. 26). Our other tests show that the switching and forming processes in all types of the devices are bias-polarity independent (Fig. 27). Since all the devices are asymmetric in structure with non-metallic substrates of either Si^{++} or TiN/Si, metal filament formation is less likely to be responsible for the observed switching because such a process usually

involves metal ion migration or injection from the electrode, which is bias-polarity dependent.[13] Moreover, metal filaments generally have higher ON current levels than those we observed here. All the observed characteristics resemble those in the M/SiO/M system,[20] where SiO plays the essential switching role. In our structures we suggest that nonstoichiometric SiO_x at the edges of the etched oxide is the switching medium. While M/SiO/M systems were first studied decades ago, the detailed underlying switching mechanism remains largely unknown and debatable.[20] The layered structure of SiO in the M/SiO/M system along with comparatively large and smooth currents contributed from the entire SiO layer makes it challenging to discern whether the switching is a bulk effect or is localized.

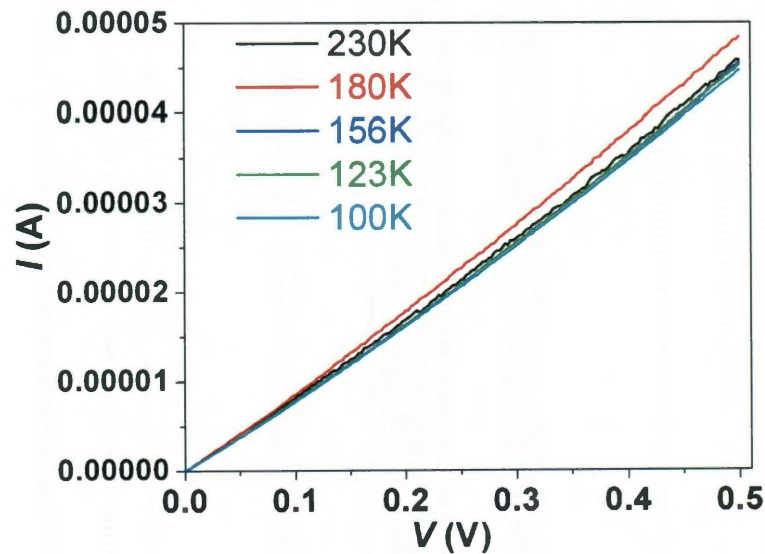


Figure 26. Temperature dependence of ON-state conduction in an electroformed $W/Ti/SiO_x/Si^{++}$ device. The data shows little temperature dependence down to 100 K.

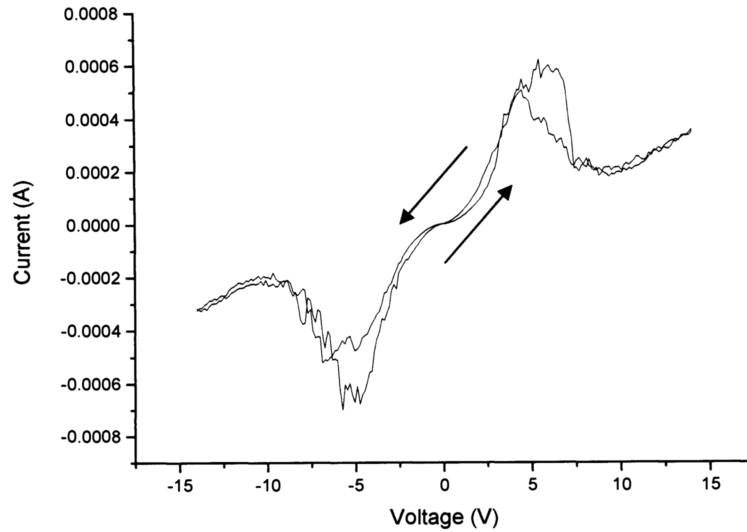


Figure 27. Polarity-independent switching *IV* curves (-15 V → + 15 V → -15 V) from a W/TiN/SiO2/TiN device.

The surface-restricted switching in our system may offer new insights. As discussed before, the *IV*s in DEVs 1-3 mainly differ in the current magnitudes and noise features. As shown in Fig. 25c, with the decreasing of the operating current level, the current fluctuations in the writing bias region increase (consider, for example, the large rises and drop in currents as the largest fluctuations). Note that in Fig. 25c the OFF current of DEV-2 is much larger than that of DEV-1, changing from a relatively smooth *IV* into one with discrete steps. We suggest that this is a consequence of having an ensemble of conducting paths in DEV-2 and only a few paths in DEV-1. The variation in switching voltages even in the same DEV-1 by different sweeps further indicates the discrete nature of conduction paths. One can

imagine that a large number of DEVs-1 in parallel would collectively reproduce the comparatively smooth *IV* in DEV-2 due to a variety of current rise and drop edges. The *IV* of DEV-3 in Fig. 25c is consistent with this idea, with an intermediate conductance device DEV-3 having features between the two limits of DEV-1 and DEV-2. These features further support discrete-path or filamentary conduction in our system at nonstoichiometric device edges, in accordance with expectations based on studies of M/SiO/M devices by different methods.[67,68] And this filamentary revelation through *IV* behaviors is also consistent with the same conclusion indicated by intermediate states in horizontal nanogap systems (see Fig. 16). It is straightforward to expect that while a large number of filamentary paths with non-uniform writing/erasing biases would limit the overall ON/OFF ratio, reducing the path number can push this ratio up, as demonstrated in DEV-1 with an ON/OFF ratio > 10^4.

3.2-4 Summary

We have demonstrated reproducible resistive switching with memory properties in vertical sandwich structures with SiO_x as the switching layer. The electrical characteristics depend significantly on the oxide etching method, as well as annealing history in reducing environment and oxide growth method. These traits suggest that the switching is filamentary in nature and takes place in the stoichiometrically poor edges of the etched oxide. The localized character of conducting paths and critical role of etched oxide surfaces raise the possibility of nano-scale SiO_x based memory,

though an improved understanding of the detailed switching mechanism would be essential. The question of the formation of individual conduction path remains open. The heat-assisted electroforming processes in our devices and the non-working state at low temperature may indicate a fusion-and-reforming mechanism induced by local heating due to hot electrons.

3.3 Resistive Switching in Metal-Free polySi-SiO_x-polySi Structures[69]

The metallic electrodes used in the vertical memory units discussed in Section **3.2** can give rise to the conjecture that metal filaments could be involved in the switching mechanism. Even in the planar nanogap structures discussed in Chapter **2**, metal electrodes have been always involved, either directly defining the nanogap (*e.g.*, W-W nanogap in Section **2.2-1**) or serving as electrical contacts (*e.g.*, carbon-material-based nanogap systems). To further elucidate that the resistive switching is not metal or carbon related,[47,49] a metallic nonmetal other than carbon forms is desirable as the electrode material. On the other hand, from the device perspective, the industry may prefer a less metal-involved process or even a metal-free protocol. A viable candidate is doped polysilicon (polySi). Therefore the following discussion focuses on resistive switching in SiO_x using polySi as both top and bottom electrodes.

3.3-1 Fabrication

The fabrication of vertical polySi-SiO_x-polySi devices starts with wafers with layered structures on a silicon substrate (Freescale Semiconductor, Inc.; see schematic in Fig. 28). A thin layer of SiO_x (40 nm, x = 1.9-2) is sandwiched between two *p*-doped polySi layers (70 nm thick, ρ = 0.005 Ω·cm; $7\times10^{15}/cm^2$ @ 5 KeV, boron) that are to be served as the top and bottom electrodes, respectively. Circular Cr masks with diameters of 50 μm (30 nm thick) were defined by standard photolithography, sputtering and lift-off processes. Reactive ion etching (RIE) was then adopted for etching. Specifically, SF_6 was used for polySi etching (RIE power: 100 mW, SF_6 flow rate: 10 sccm, pressure: 30 mTorr, etching rate ~ 70 nm / min) and O_2/CHF_3 was used for SiO_x etching (RIE power: 150 mW, CHF_3 flow rate: 25 sccm, O_2 flow rate: 15 sccm, pressure: 100 mTorr, etching rate ~ 40 nm / min). After the top polySi layer etching and the SiO_x layer etching, the Cr masks were removed by Cr etchant solution (CEP-200). The chosen diameters of the devices (50 μm) are for an easy probe-tip landing (see schematics of device & electrical testing setup in Fig. 29 a, b). Electrical characterizations were performed at room temperature in vacuum (10^{-5} Torr), unless otherwise specified.

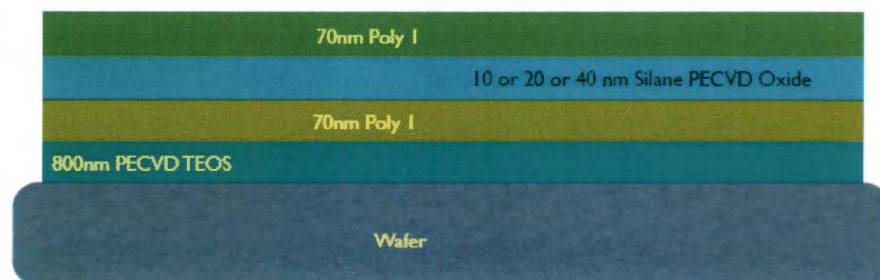


Figure 28. Schematic of the layered structure of polySi-SiO_x-polySi wafer.

3.3-2 Memory Switching and *IV* Curves

The typical current-voltage relationship shows resistive switching behavior featuring conductance jump and drop at ~ 3.5 V and ~ 8 V, respectively (blue curve in Figure 29c). The voltages at these two events define the set and reset regions as indicated in Figure 29c. For example, a voltage pulse (+6 V) in the 'set' region switches the device into a low-resistance (ON) state whereas a voltage pulse (+13 V) in the 'reset' region switches the device into a high-resistance (OFF) state (inset in Figure 29c). The programmed states are nonvolatile and can be read nondestructively in the 'read' region. Figure 29d shows a series of switching cycles with an ON/OFF ratio $>10^5$, which is also inferred in the hysteretic *IV*s in Figure 29c. The switching behaviors observed in the above polySi-SiO_x-polySi structures are very similar to those observed in other SiO_x-based systems adopting metal/carbon electrodes discussed in chapter **2** and section **3.2**. Since the elements involved in this structure are oxygen and silicon, it further indicates that the switching is not metal- or carbon-related. The devices yield can be very high (*e.g.*, > 90%). In fact, for the very recent series of samples prepared for cosmic-radiation resilience test, a yield of over 99% (200 devices out of 201 devices) was achieved (see Appendix for details). The high yield in the devices discounts the possibility of extrinsic effects from contaminations other than the SiO_x and polySi components.

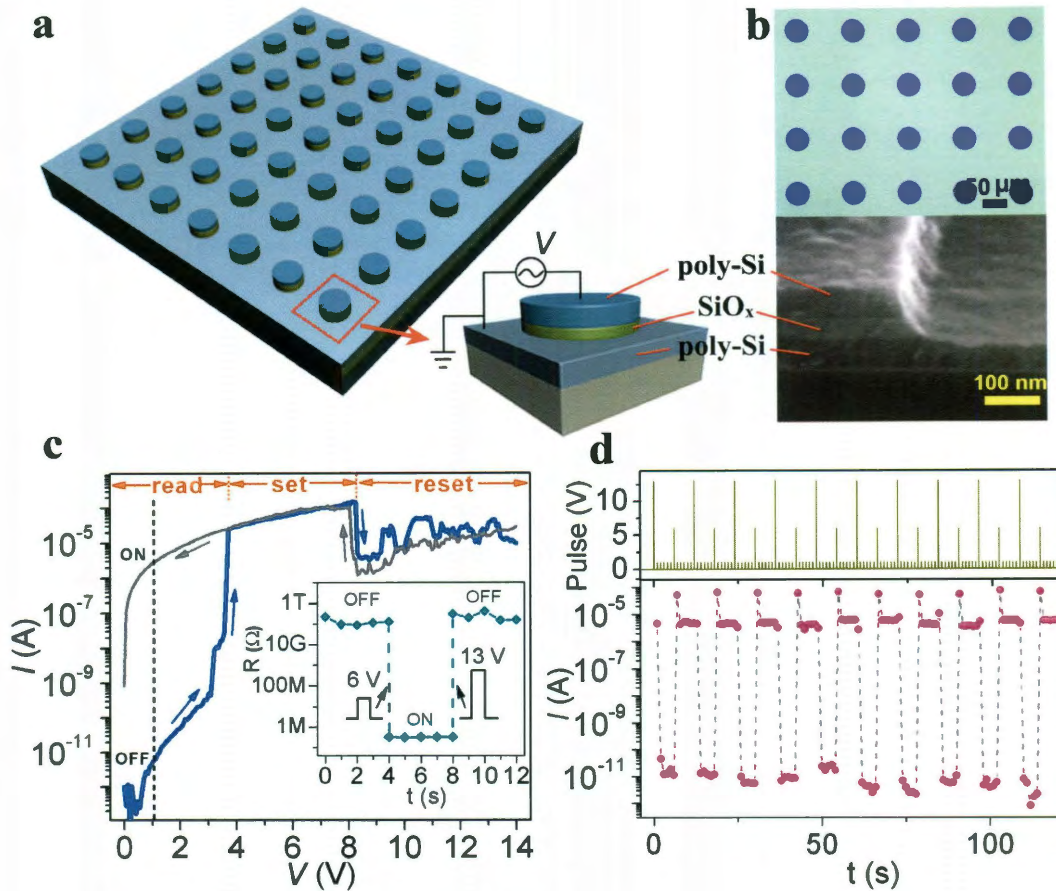


Figure 29. Device structures and electrical characterizations. (a) Schematics of the poly-Si/SiO_x/poly-Si devices (50 μm diameter) and the electrical characterization setup. (b) An optical top-view image of the device arrays (top panel) and a SEM image of the cross section (bottom panel). (c) Characteristic *IV*s in a formed device: (blue curve) starting from an OFF state, the conductance of the device suddenly increases at +3.5 V and drops at +8 V. During a subsequent reverse voltage sweep (gray curve), the conductance goes back to a higher value at +8 V, producing a current hysteresis. Corresponding 'read', 'set', and 'reset' regions are defined based on these conductance changes. The vertical dashed line indicates the ON/OFF ratio at 1 V. Inset: device resistance changes after +6 V and +13 V programming voltage pulses. (d) (Top panel) A series of voltage pulses of +13 V, +1 V (5 times), and +6 V serve as reset, read (5 times), and set operations, respectively. (Bottom panel) currents corresponding to each voltage pulse in the top panel.

3.3-3 Metal-Free Fabrication Process

Strictly speaking, a metal element could still be present in the polySi-SiO_x-polySi devices described above since the fabrication process involves a Cr mask. To avoid this concern, polySi-SiO_x-polySi devices were also fabricated by a metal-free process using photoresist (Microposit S1813) as sacrificial masks. At a spinning rate of 3000 rpm, the coated photoresist (thickness > 1 μm) is sufficient to protect the polySi and SiO_x layer underneath during RIE etching. Wet etching of SiO_x by BOE was also used as a variation in the fabrication flow in order to further clarify that the switching behaviors are not related to contamination introduced during the fabrication process. Fig. 30a shows the schematic of the metal-free fabrication process. Fig. 30b shows the typical memory switching in a polySi-SiO_x-polySi device fabricated by the metal-free process.

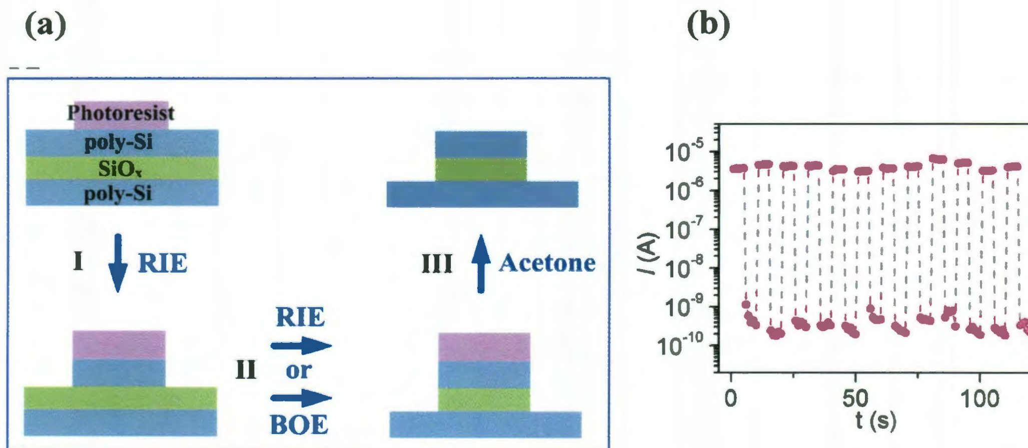


Figure 30. Variation in device fabrication and memory switching. **(a)** A schematic of the flow of device fabrication. Photoresist (S1813) was first patterned as a sacrificial

mask by standard photolithography. A RIE process was then performed to etch away the top poly-Si layer (step I) using SF_6 as the recipe. The etching of SiO_x layer can use either a wet- or dry-etch method (step II). For the dry-etch method, RIE with a protocol of CHF_3/O_2 was adopted. The dry-etch method is anisotropic and produced little undercut (as shown in Fig. 1b in the main letter), and was adopted for the all the devices described in the main letter. For the wet-etch method, BOE was used to remove the SiO_x layer, leaving the part underneath the poly-Si electrodes protected. Due to the isotropic etching of HF, an undercut was usually produced in the SiO_x layer in the devices. However, this undercut did not affect the stability of the structure (*i.e.*, the poly-Si layer did not collapse at the edge region) because the thickness of SiO_x layer was relatively thin (40 nm) compared to that of the top poly-Si layer (70 nm). Once the structure was defined, the photoresist mask was removed by acetone (III). (**b**) While the dry-etch method (RIE) was exclusively adopted for devices discussed in the main letter, devices fabricated by the wet-etch method (BOE) were also fabricated here to exclude the possibility of contamination-related switching at the SiO_x vertical edge introduced during the etching step. The same memory switching in a poly-Si/SiO_x/poly-Si device by the wet-etch method is shown here, using +1 V (5 times), + 6 V, and + 13 V as read, set, and reset operations, respectively. Programming currents are not shown.

The reason that the Cr-mask etching process is more frequently used is that: (1) The photoresist mask (> 1 μm) is much thicker than the Cr mask (~ 30 nm) and there is a potential shadowing effect from the photoresist mask during the RIE etching, resulting in a less well-defined vertical edge. (2) The RIE gases react with the photoresist and produce a layer of resilient material that is difficult to remove (Fig. 31). The stripping-off process of photoresist after RIE etching should be as follows:

rinse the devices (~ 5 s) in acetone solution that is being ultra-sonicated to first remove the residual layer on the photoresist surface and then put it in acetone solution for the complete removal of the photoresist.

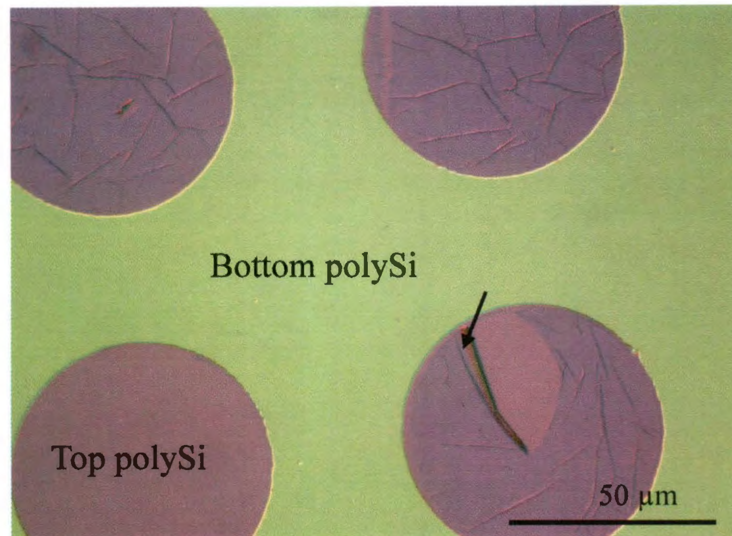


Figure 31. A layer of resilient material (indicated by the arrow) was left after the RIE etching of photoresist-masked polySi-SiO_x-polySi devices which were washed in acetone (without pre-ultrasonication). Note that once the layer of material is in direct contact with the polySi electrode, it is difficult to remove even by ultrasonication. This is why the pre-ultrasonication described above is important. A 5 s pre-ultrasonication is enough. Longer ultrasonication may harm the layered device structure.

3.3-4 Forming Processes and Implications

Similarly, an electroforming process is always involved in order to convert the pristine non-conducting polySi-SiO_x-polySi device into a resistive switching state. As described in Section **3.2-3**, this process usually involves limited current or voltage

stress, in which a soft breakdown is induced. Here this electroforming is achieved similarly by a voltage sweep to a high value, within which large current fluctuations take place. Continuous voltage sweeps by gradually reducing the voltages while maintaining the current fluctuations lead to the switching (Fig. 32). The forming process can also be done by continuous voltage pulses instead of voltage sweeps. Generally, one can use the memory cycling process for the pulse forming: keep the writing/set voltage unchanged during the entire process while only adjusting the magnitudes of erasing/reset voltage pulses; increase the magnitude of the erasing pulse until a certain programming current level (10^{-6} A) is reached; then quickly reduce the erasing/reset pulse magnitude while still keeping the similar reset current level until the magnitude of the reset pulse reduces to the normal working voltage range (Fig. 33).

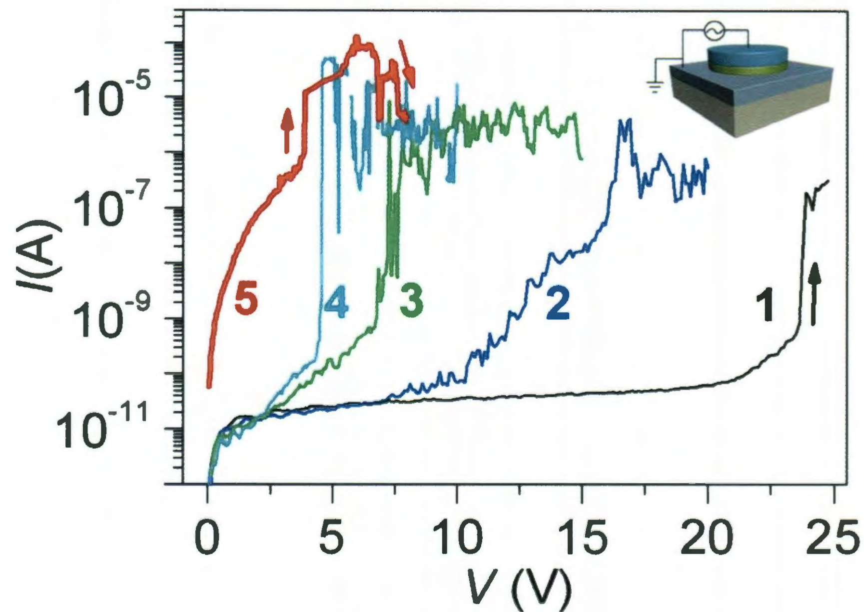


Figure 32. A typical forming process in a vertical poly-Si/SiO_x/poly-Si device prior to

annealing. The device structure (top inset) is the same as described in Fig. 1 in the main letter. The numbers near the *IV* curves indicate the corresponding sweep order. The device was in a non-conduction state initially. By voltage sweep to a high value (*e.g.*, +25 V, black curve), a sudden current increase (to ~ 10^{-6} A) was induced (indicated by the black arrow), accompanied by current fluctuations. During the subsequent voltage sweeps (curve 2-4), the currents gradually increased as well as the current fluctuations. And a characteristic resistive switching *IV* (red curve) then appeared, featuring the sudden current increase and drop (indicated by red arrows).

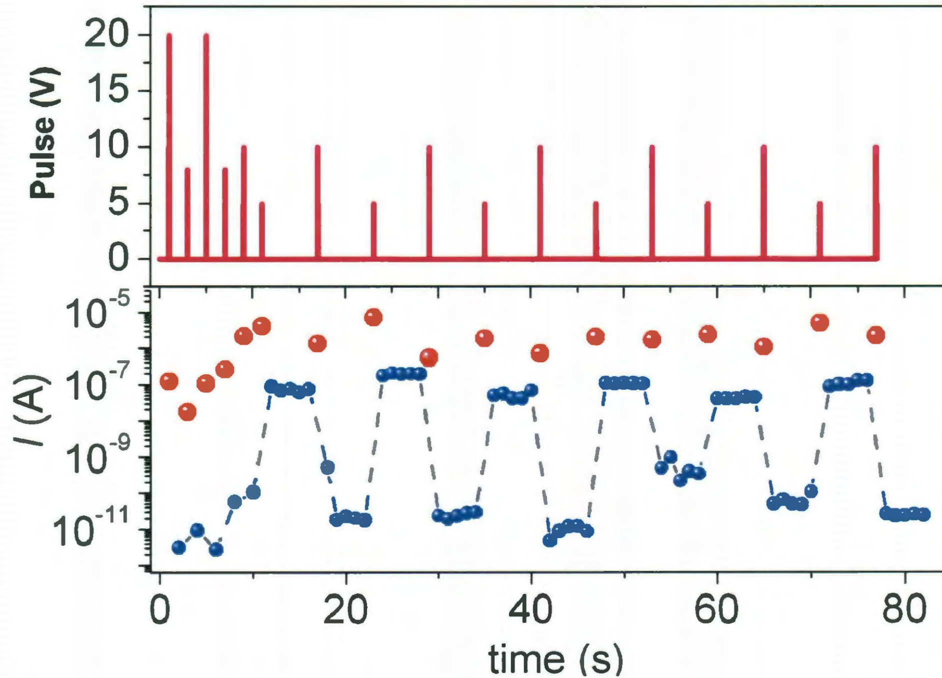


Figure 33. Pulse-electroforming processes in a polySi-SiO_x-polySi device (40 nm SiO_x by wet etching). Top panel shows the programming/forming pulses. Bottom panel shows the corresponding programming current (red dots) and the conductance state (blue dots, read at +1 V).

As described in Section **3.2**, thermal annealing is found to assist the electroforming process by reducing the initial soft breakdown voltage in the pristine polySi-SiO_x-polySi devices (Fig. 34). The annealing here was done between 450 °C – 600 °C in either vacuum (< 150 mTorr) or a reducing environment (Ar/H_2). Generally, the reducing environment induces higher initial conduction in the devices compared to those annealed in a vacuum environment (Fig. 35). Higher temperature further reinforces this trend.

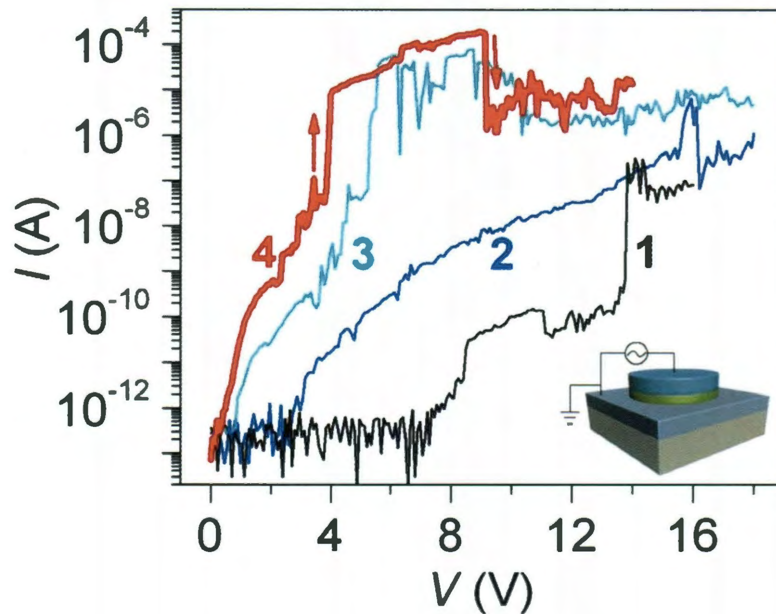


Figure 34. Annealing-assisted forming process in a vertical poly-Si/SiO_x/poly-Si device (40 nm SiO_x). An additional thermal annealing process was performed before the electrical characterizations. The annealing was done at 600 °C for 10 min in vacuum (140 mTorr). The numbers near the *IV* curves indicate the sweep order. After the thermal annealing, the initial conduction increase was induced at a lower voltage value (at ~ +8 V, indicated by black arrow in curve 1). More examples can be found in the following Fig. 35a. As a result, the forming process could be initialized at a lower voltage (< 20 V here compared to > 20 V in Fig. 32). *IV* curves 2-3 are the subsequent

voltage sweeps that feature the similar trend of gradual increases in conduction and current fluctuations, until the characteristic *IV* (curve 4) was formed. For as-made devices without thermal annealing, more than 6 voltage sweeps were usually involved in the forming process to reach the final switching state. In the thermally annealed structures, 3-6 voltage sweeps were usually needed. The initial voltage sweep needs to attain a voltage level whereupon there is a sudden current increase to ~ 10^{-6} A as seen in curve 1.

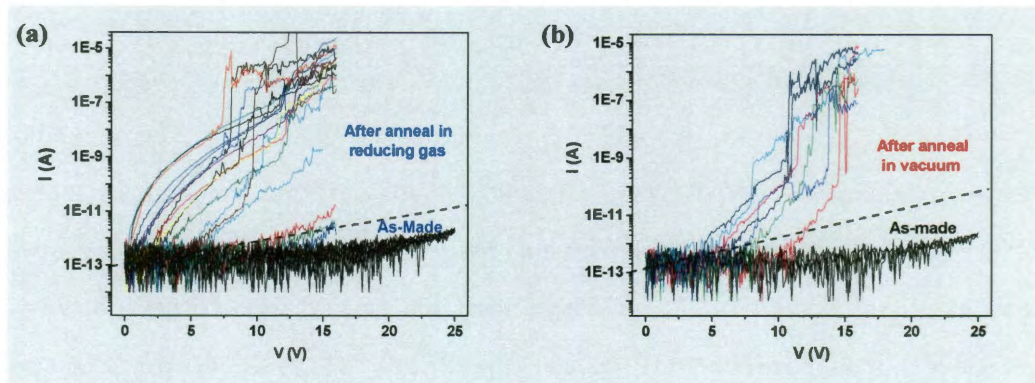


Figure 35. Control tests of initial conduction increases in polySi-SiO_x-polySi devices (40 nm SiO_x) after annealing for 10 min at 600 °C in (a) reducing environment (Ar/H_2) and (b) vacuum (150 mTorr) environment. The black curves show the conduction before the annealing and the color curves show the conduction after the annealing.

The annealing-assisted forming process helps to track the location of initial conduction or the electroforming site. A control experiment was done in two groups of devices. One group has the same structure as depicted in Figure 29a with an etched vertical defined SiO_x edge. The other group has all the same parameters except that no vertical edge was made in the SiO_x layer (Fig. 36b). After annealing under the same conditions, the first group showed a conductance increase that led to the forming

process, whereas no conductance increase was observed in the second group (Fig. 36b). This control test shows that the forming process is related to the SiO_x vertical edge, as is also observed in the metal-electrode SiO_x devices discussed in Section **3.2**. It also discounts the role of dopant thermal diffusion from the polySi electrodes into the bulk SiO_x layer. In fact, the annealing-assisted forming occurs at a temperature as low as 400 °C, a temperature too low for dopant diffusion.[70] It should be noted here that since the forming process is SiO_x-surface or SiO_x-edge related, it is expected that different etching process may lead to different SiO_x surface morphology/stoichiometry, thus affecting the forming process. For example, in general wet-etch-defined defined SiO_x vertical devices are easier to electroform, with fewer voltage sweeps being required than in dry-etch-defined devices. The actual cause for this is not yet clear. It may be due to different SiO_x surface chemical termination or morphology after the different etching methods. In this regard, a 5 s rinse in BOE for the dry-etch-defined polySi-SiO_x-polySi devices may help ease the forming process, and also removes the surface native oxide on the polySi electrodes. Since HF etching of SiO_x is isotropic, prolonged BOE etching of SiO_x causes large undercuts and reduces the device reliability.

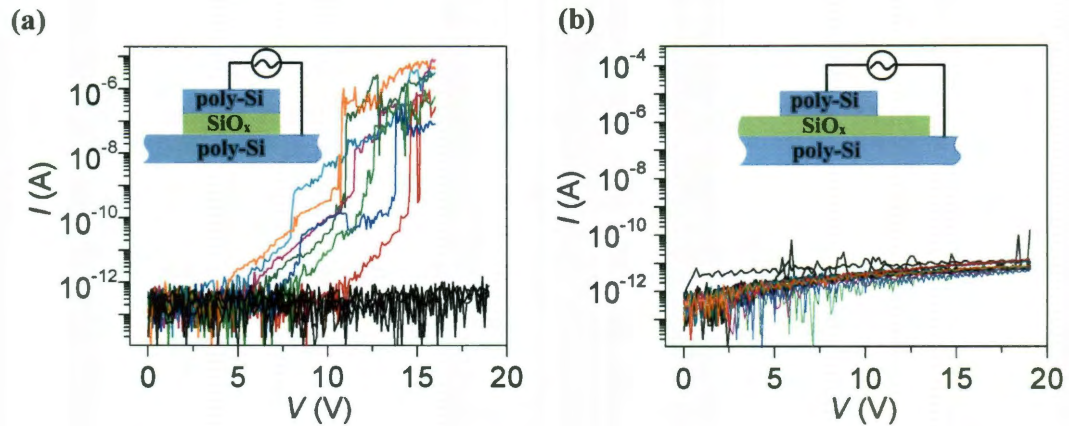


Figure 36. Annealing effects in devices with and without a SiO_x vertical edge. (a) Initial conductions in different devices before (black curves) and after (color curves) annealing at 600 °C for 10 min in vacuum (140 mTorr). The inset is a schematic of the structure of the device (side-view) which is the same as depicted in Fig. 29 in the main letter. Substantial current increases and fluctuations were observed after the annealing. (b) Annealing effects on the initial conductions in devices without a SiO_x vertical edge. The inset shows the device structure (side-view). All the parameters of the devices and fabrication process are the same as in (A), except that no etching step was performed in the SiO_x layer. After annealing under the same conditions, *i.e.*, at 600 °C for 10 min in vacuum (140 mTorr), the devices in this configuration showed no increase in the conduction (color curves) compared to those prior to annealing (black curves).

3.3-5 Protrusion and Pore Structure

With the likelihood of edge-related forming, we further devised a protrusion structure that has a limited SiO_x vertical edge while still permitting an easy probe-tip landing (Figure 37a, b). The confined vertical edge facilitates direct monitoring of the forming process. After the forming process that led to the switching, observable

protrusion structure with limited SiO_x vertical edges at the protruding region. The top inset shows the schematic of the structure. (b) An enlarged SEM image of the protruding region after a 10-min annealing at 600 °C in vacuum, prior to the electrical forming process. (c) A SEM image of the same protruding region in (b) after the forming process that led to the switching state. The blue arrow indicates morphology changes in the SiO_x layer. (d) A schematic of a cross-sectioned pore structure (top panel) and the actual top-view SEM image of a pore structure (bottom panel). (e) Memory states (read at +1 V) during a series of cycles in the pore structure. (f) ON currents with respect to the diameter of the SiO_x vertical edge. The data point at 50 μm is from pillar structures in Figure 29a and the others are from pore structures with different diameters. The thicknesses and material compositions of the SiO_x and poly-Si layers in the above structures are the same as those adopted in Figure 29.

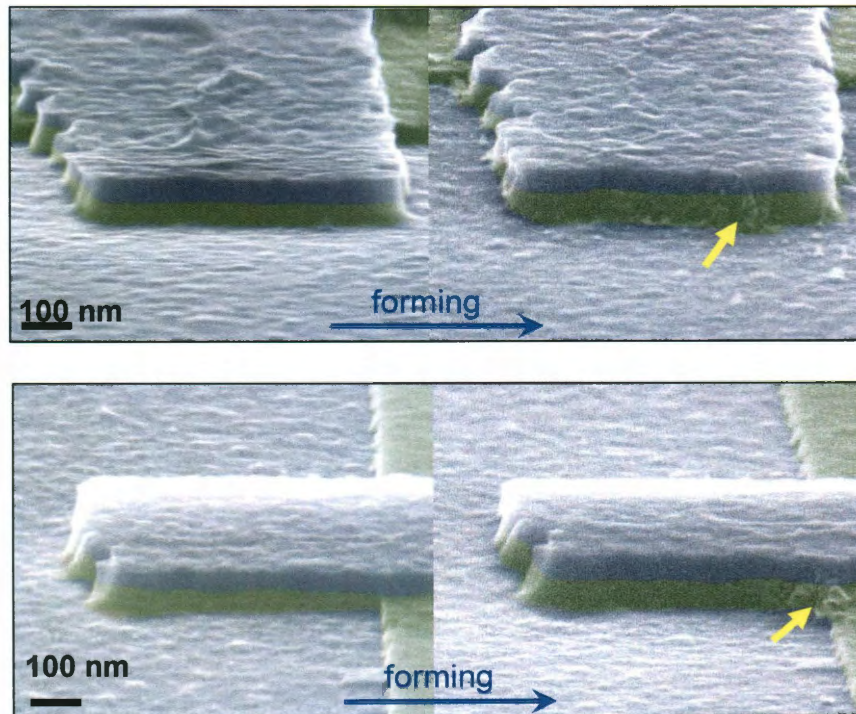


Figure 38. Examples of morphology changes in the SiO_x layer at the vertical edge region after electroforming.

A complementary embodiment was fabricated where the SiO_x vertical edge is placed the inner surface of the pore (Figure 37d, also see the fabrication scheme in Fig. 39). The edge-induced forming localizes the switching (Figure 37e) around the pore region. By varying the pore diameters, current scaling properties were also investigated. Notably, the ON current level stayed the same while reducing the diameter from 50 μm to 200 nm (Figure 37f). This indicates that the switching happens locally instead of uniformly along the entire circumference, which can also be inferred from the localized morphology changes in the SiO_x layer in Fig. 38. This is also desirable for the construction of fully CMOS-compatible reprogrammable vias[73] to ensure acceptable current passage as the via sizes scale.

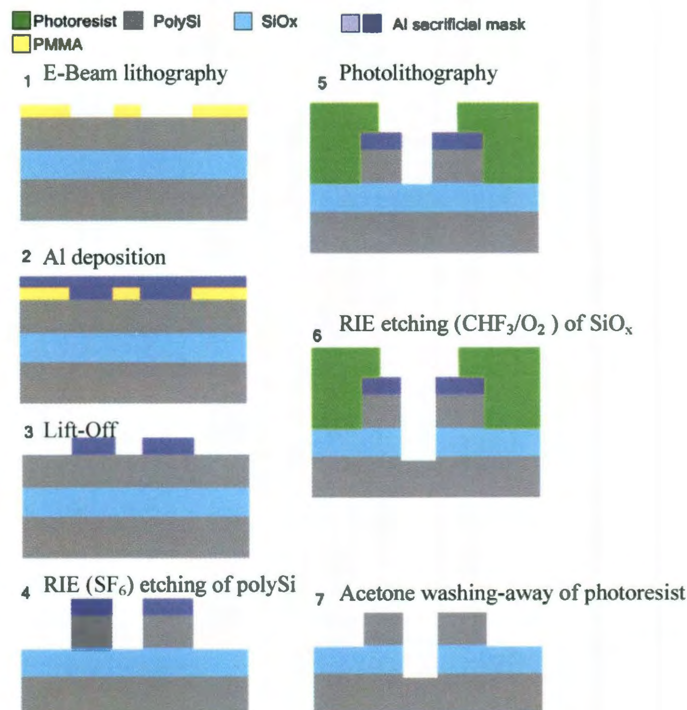


Figure 39. Schematic of the fabrication process for the pore structure. A similar process can be adopted to fabricate the protrusion structure in Fig. 37a.

3.4 Memory Properties

In this section, various properties of the resistive switching in SiO_x are discussed. These properties serve the purpose of potential device-performance projections as well as providing mechanistic implications.

3.4-1 Retention

One of the most important characteristics for nonvolatile memory applications is the data retention time. For this characterization, two groups of polySi-SiO_x-polySi (40 nm SiO_x) devices with one group set into ON states and the other OFF states were kept in an ambient environment for three months. Fig. 40 shows the testing results. Both the ON and OFF states largely retained their conduction states.[74] Specifically, a slight reduction in the conductance in the ON states was observed. However, this may not reflect the actual conductance reduction from the SiO_x. As the electrodes are polySi, native-oxide effect is always present during the memory-state readout (read at +1 V). For the initial memory-state readout, since it immediately followed the higher-voltage programming processes, the surface-oxide effect was absent: the programming voltage already removed the oxide barrier between the probe tip and the polySi through electrical breakdown. However, for the second memory-state readout,

no programming process was involved and a native-oxide barrier may have built up between the polySi electrodes and the probe tips. For this reason, this conductance decrease was observed by simply lifting the probe tip up and landing it down again on the same top polySi electrode, during which the probe tip moved to a different place on the native-oxide layer. It is suggested that during the second memory-state readout, one could first remove the oxide barrier between the bottom polySi electrode and the probe tip by placing the two probe tips on the same bottom polySi layer and sweeping the voltage to a high value. Then one probe tip could be fixed while using the other probe tip to contact the top polySi electrode. The probe tip in contact with the top polySi electrode may need to be moved to several locations with the memory state constantly monitored during the readout process. The actual conductance of the SiO_x device should be close to the maximum and stable value during this process. A general trend of increased conductance in the OFF states is seen in Fig. 40 (bottom panel). Since the OFF-state conduction is largely through tunneling and the conducting site is at the vertical SiO_x edge, it is likely that moisture or other adsorption may substantially affect the conductance.

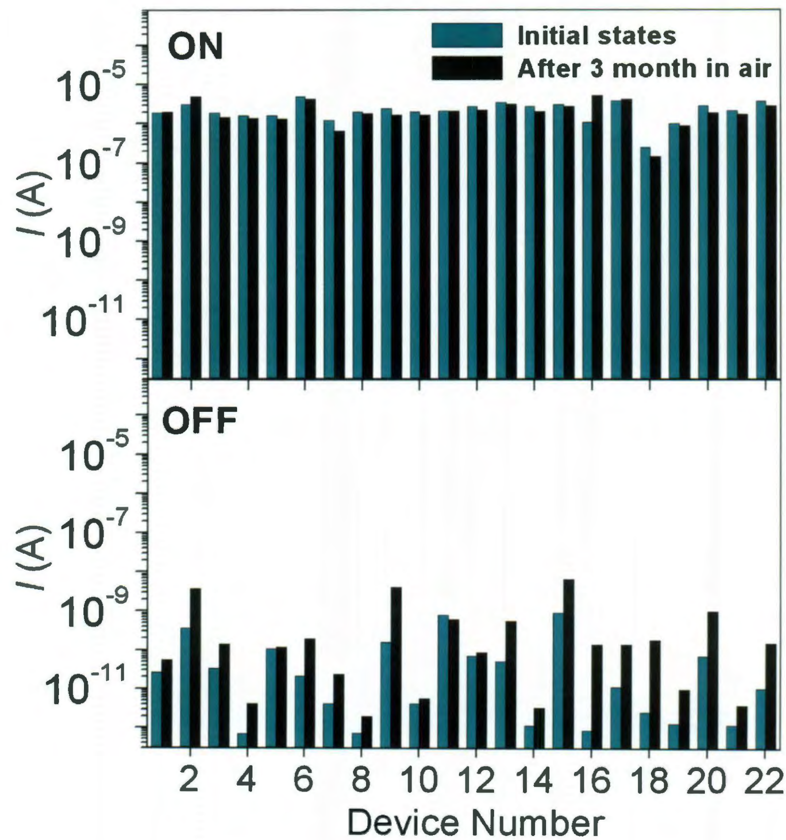


Figure 40. Memory-state retention in polySi/SiO_x/polySi devices. (**a**) ON states from 22 individual devices after 3 months in ambient environment. (**b**) OFF states from 22 individual devices after 3 months in an ambient environment.

The SiO_x memory devices also feature nondestructive reading. At +1 V, the memory states can be continuously read 10^5 times without degradation (Fig. 41a). It also indicates an extrapolated retention beyond 10 years. This nondestructive reading holds for memory states at various conductance stages (Fig. 41b). It should also be noted that while the memory states are stable in an ambient environment, the memory programming process needs to be in an oxygen-deficient environment. In particular,

the erasing/reset operation can be done in an ambient environment whereas the writing/set operation cannot be performed in oxygen (Fig. 42). The OFF device can still be activated into a switching state when placed back in a vacuum environment. Further study is needed to determine the oxygen/pressure tolerance for the memory programming.

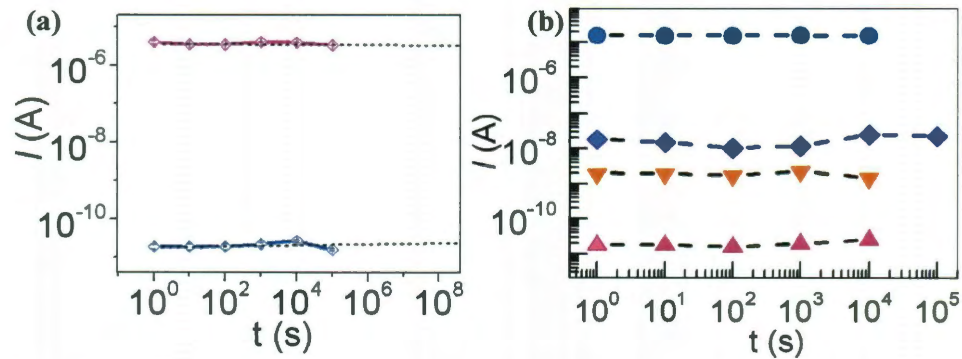


Figure 41. Memory reading cycles for different memory states. (a) 10^5 memory reading cycles for the ON and OFF states. The doted line indicates the extrapolation. (b) 10^4 or 10^5 memory reading cycles for memory states and different conductance states. The memory states were recorded by voltage pulses at a rate of 1 read per sec. All the memory states were read at + 1 V.

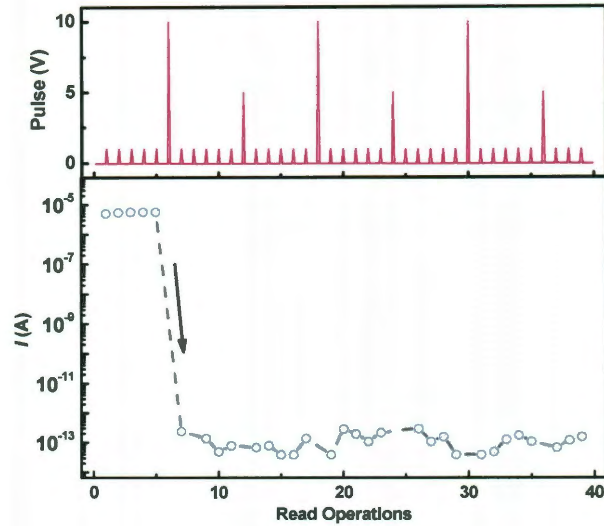


Figure 42. Memory cycling test in ambient environment showing that an erasing/reset voltage can reduce the conduction but the writing/set voltage pulse does not set the device back to an ON state.

3.4-2 Thermal-Annealing Effects on the Memory State

The detrimental role of air/oxygen during programming indicates that oxidation processes during current local heating hinders the memory switching (in particular, from OFF to ON). This is consistent with the annealing effect on the programmed device states (Fig. 43). A drastic conductance reduction was observed in the ON states after the devices were annealed in an ambient environment at 700 °C for 10 min. The thermal annealing in ambient environment not only destroys the memory state, but also deactivates the device into a non-switching state. A similar re-electroforming process is generally involved before the device starts memory switching again in a

reduced pressure (10^{-5} Torr, Fig. 44). This effect is more prominent in devices with thinner SiO_x (20 nm, Fig. 44a) than that with thicker SiO_x (40 nm, Fig. 44b).

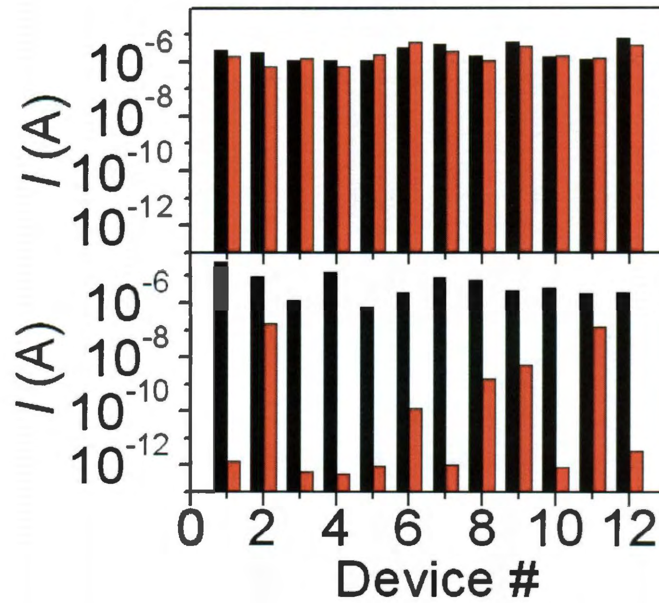


Figure 43. Conductance states (read at +1 V) in devices before (black column) and after (red column) annealing at 700 °C for 10 min in Ar/H_2 environment (top panel) and in air (bottom panel).

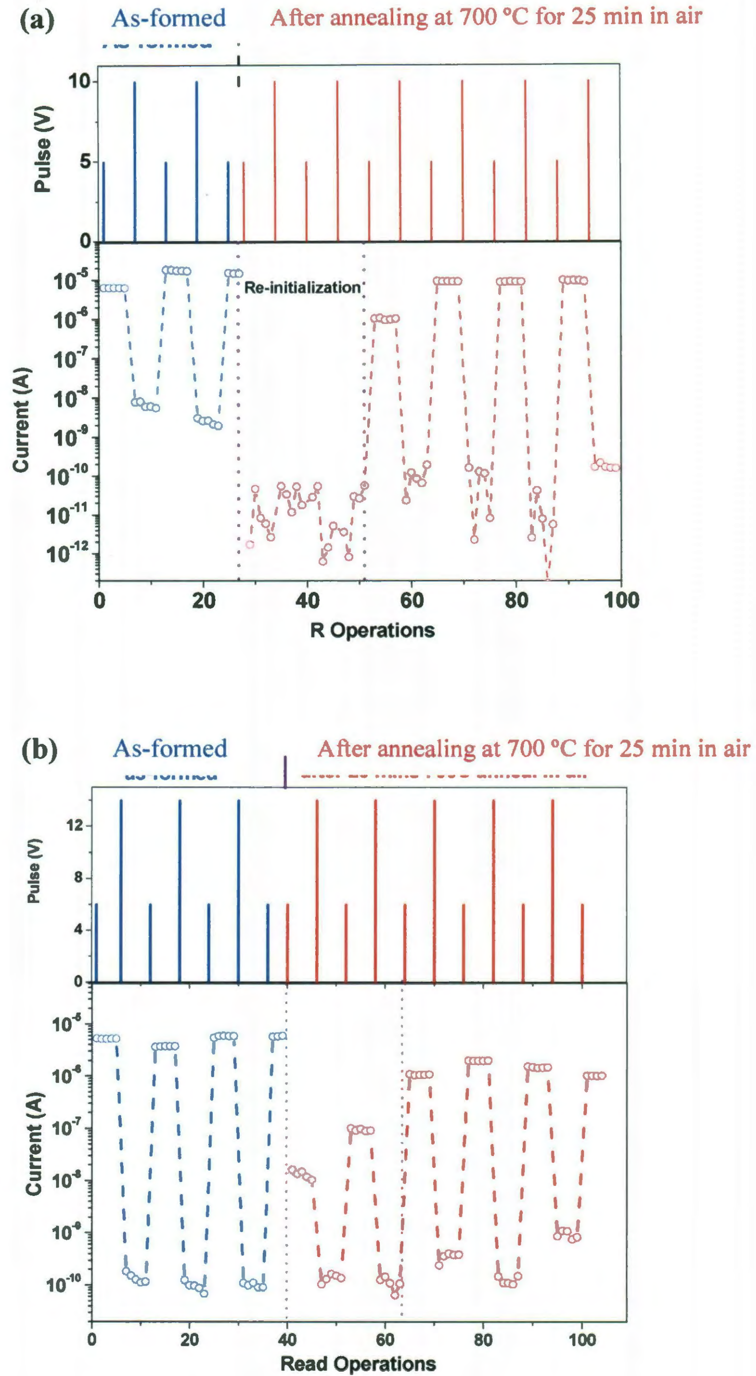
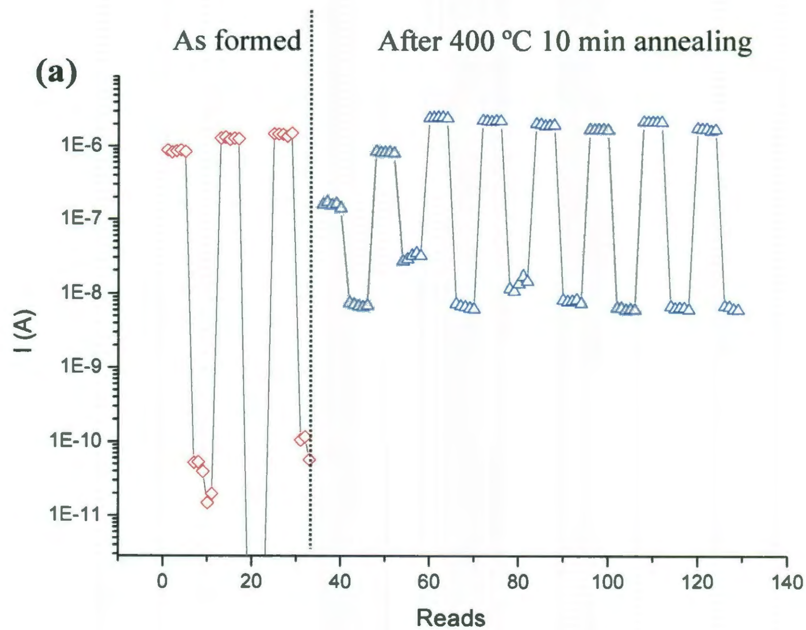


Figure. 44. (a) Memory cycling in vacuum environment in a polySi-SiO_x-polySi device (20 nm SiO_x) before (blue region) and after (red region) ambient atmosphere annealing (25 min, 700 °C). (b) Memory cycling in a 40 nm SiO_x device annealed under the same conditions as in (a). The devices were fabricated by the wet-etching

method.

Although annealing in reducing environment does not substantially alter the ON conductance (top panel in Fig. 43), it changes the switching property of the device. As shown in Fig. 45 a-c, the ON/OFF ratio gradually decreases with the increase of the annealing temperatures, mainly because of the increased conductance in the OFF states. For a prolonged (25 min) annealing at 700 °C in a reducing environment, the device suffered hard breakdown following the memory cycling attempt (Fig. 45c).



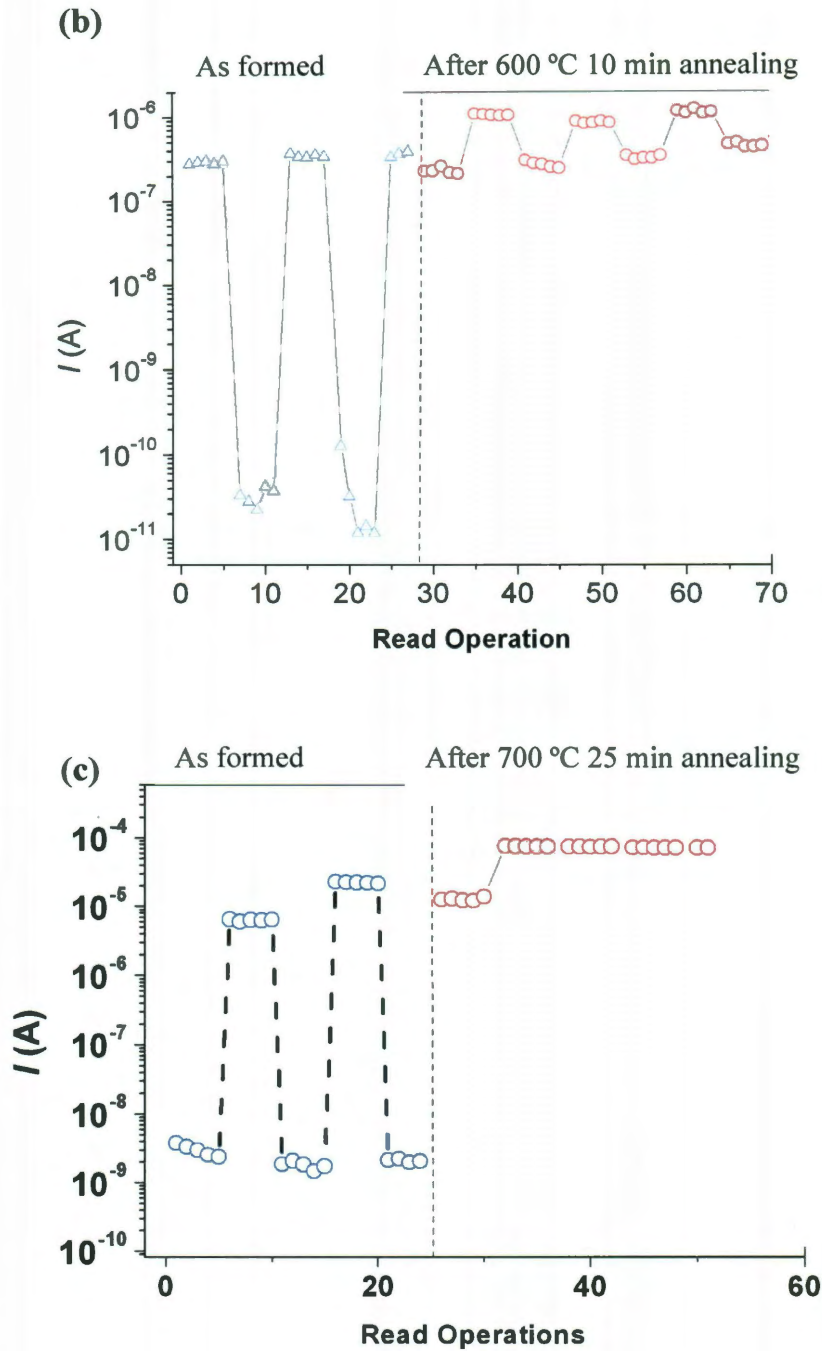
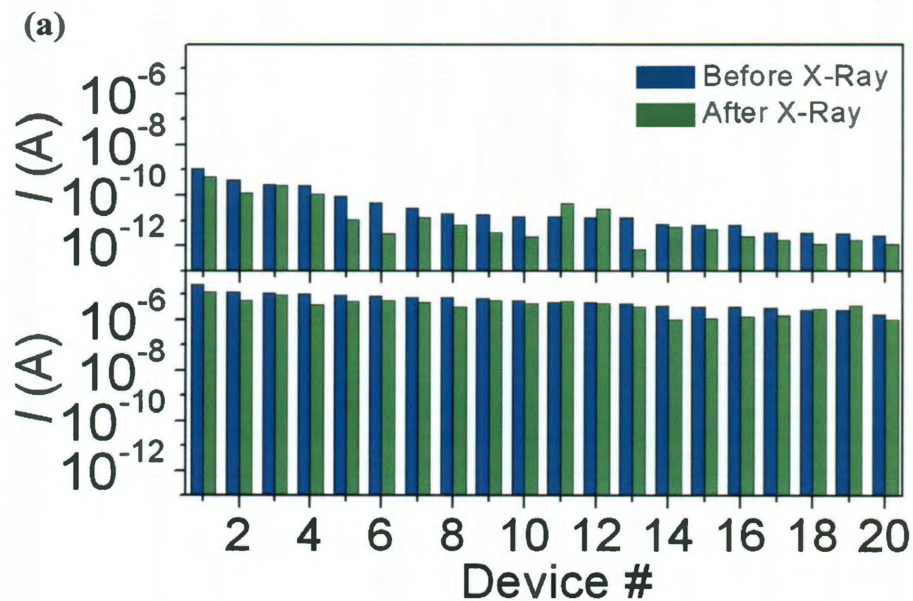


Figure 45. Memory switching in polySi-SiO_x-polySi devices (by wet-etching process) after annealing in reducing environment (Ar/H_2) at different temperatures: (a) 400 °C for 10 min, (b) 600 °C for 10 min, (c) 700 °C for 25 min.

3.4-3 X-Ray and Heavy-Ion Irradiation Tests

Two groups of polySi-SiO_x-polySi devices (40 nm), with one group set into ON states and the other OFF states, were exposed to X-ray (8 KeV, Rigaku D/Max Ultima II) for 2 h. Both the ON and OFF states tend to retain their as-programmed states (Fig. 46a), indicating robust resilience against X-ray irradiation. The devices also retained their switching properties after the X-ray irradiation (Fig. 46b, c). These tests indicate that the resistive switching in SiO_x is not likely to be charge-based as the estimated dose ~ 2 Mrad (SiO_2) is more than one order of magnitude higher than the failure level of charge-based flash memory.[75]

(a)



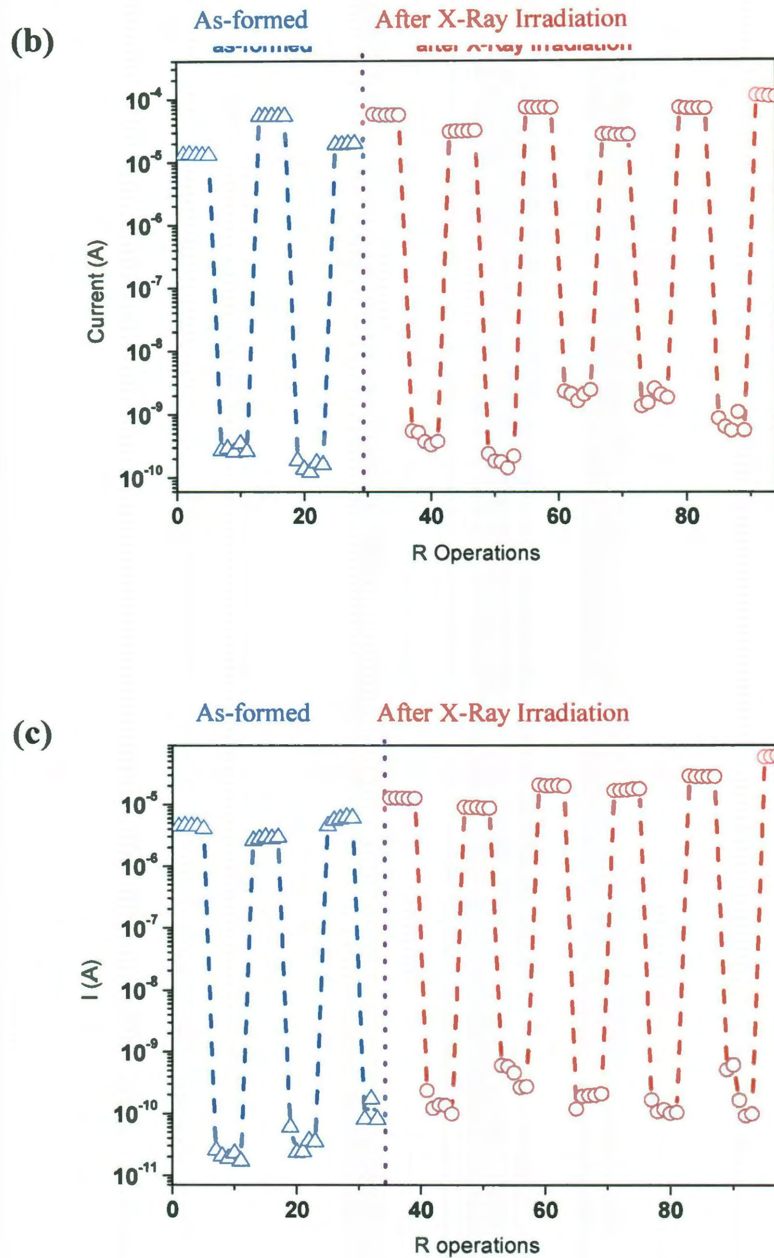


Figure 46. X-ray irradiation test. (a) Conductance states (read at +1 V) before (blue) and after (green) X-ray irradiation at a dose ~ 2 Mrad in 40 polySi-SiO_x-polySi devices, with 20 programmed to OFF (top panel) and 20 programmed to ON (bottom panel). (b) Memory switching in an ON-state device before (blue region) and after (red region) X-ray irradiation. (c) Memory switching in an OFF-state device before (blue region) and after (red region) X-ray irradiation.

SiO_x planar memory devices (α-C nanogap devices) as described in Section **2.2-2** were also used for heavy-ion irradiation test (Texas A&M University). The α-C layer was grown by CVD method[49] instead of by sputtering method.[52] 10 out of 11 ON-state devices had a slightly decreased conductance after irradiation with 1 having a slightly enhanced conductance. The conductance changes are all within the same order, so all of the devices maintained the ON states. 6 out of 8 OFF-state devices showed reduced OFF conductance after irradiation. The other 2 OFF-state devices maintained the very close conductance. Overall, both ON and OFF states all retained the conductance states after the irradiation (Fig. 47).

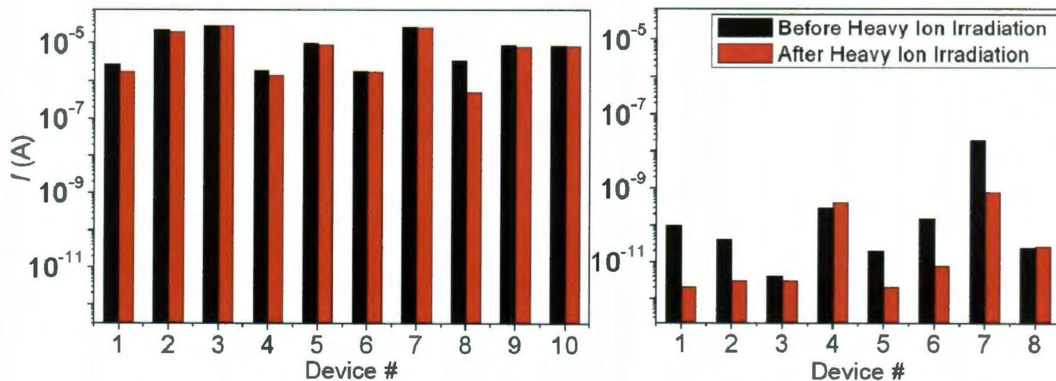


Figure 47. ON-state (left panel) and OFF-state (right panel) retention in α-C nanogap devices before (black column) and after (red column) heavy-ion irradiation.

It should be noted that the heavy ion dose was ~ 3×10^5 $cm^{-2}s^{-1}$. So a 15-min

exposure (that was the maximum time allowed for a free test from Sandia) results in an ion flux of $\sim 3\times10^8$ cm^{-2}, which is equivalent to a $_3$ ions per μm^2 for the overall irradiation. Considering that the device's functional localized filament could be much smaller than an area of 1 μm^2, the above data may not be sufficient to justify its heavy-ion resilience based on impact, but resilience predicated upon it unlikelihood of being impacted by a heavy ion.

3.4-4 BOE Etching Test

As is discussed in Section **3.3-4**, since the switching site is most likely located at the SiO_x vertical edge region, BOE etching was performed in the switching devices to gradually remove the SiO_x surface/edge for further study. Nine electroformed polySi-SiO_x-polySi devices (5 with 40 nm-SiO_x and 4 with 20 nm-SiO_x) were placed in the BOE solution for consecutive time spans of 25 s, 60 s and 105 s. The memory states and switching property were tested between the intervals. The results are summarized as follows:

(i) All 9 devices retained the ON states after 60 s BOE etching (the isotropic etching rate of SiO_x in BOE is ~ 50 nm / min; however, slower etching rate may be expected in the undercut region in vertical polySi-SiO_x-polySi device).

(ii) 4 out of 5 of the 40 nm-SiO_x devices kept switching after 60 s BOE treatment (Fig. 48 a-d). 2 of the 4 even kept switching after an additional 45 s BOE etching (Fig. 48 a-b).

(iii) All of the 4 20nm-SiO_x devices kept switching after 25 s BOE treatment. After 60s BOE etching, however, all of them became fully conductive (non-switchable state) within several cycles (Fig. 49 a-d).

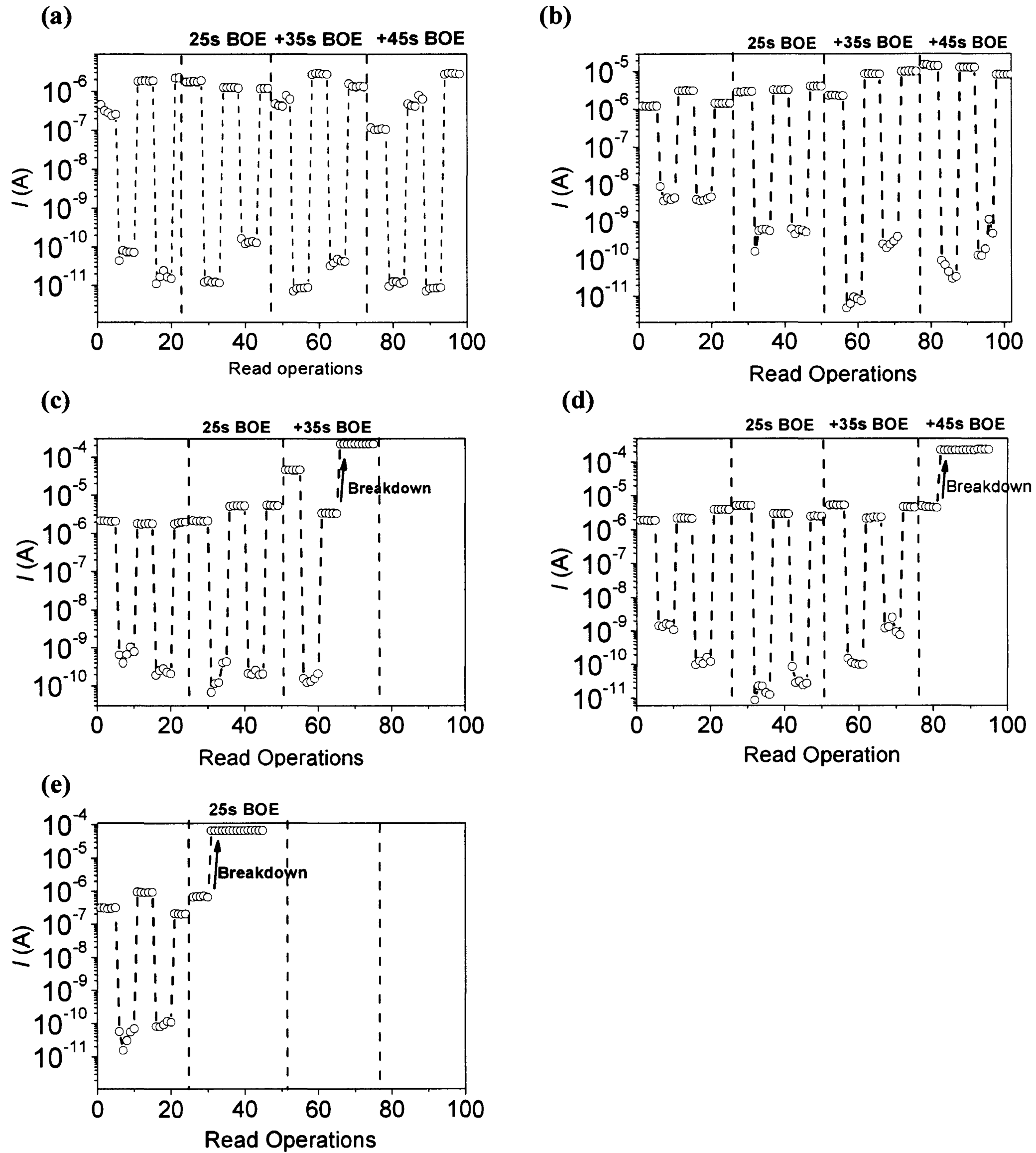


Figure 48. Memory-switching test in 5 polySi-SiO_x-polySi (40 nm SiO_x) devices after consecutive 25 s, 60 s, and 105 s of BOE etching (programming current not shown).

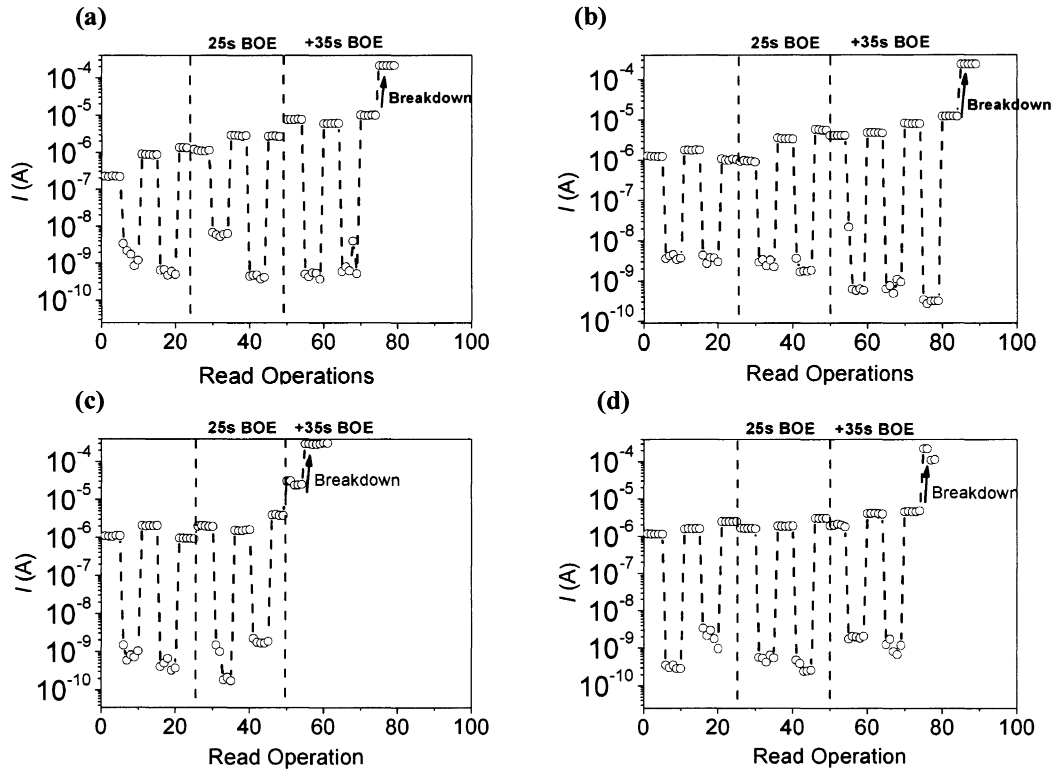


Figure 49. Memory-switching test in 4 polySi-SiO_x-polySi (20 nm SiO_x) devices after consecutive 25 s, 60 s, and 105 s of BOE etching (programming current not shown).

The above BOE-etching test in switching SiO_x devices indicates that: the switching path (filament) is not completely at surface and/or the switching region might be more resilient to HF etching.

3.4-5 Switching Speed

The continuous memory cycling tests were performed using an Agilient 4155C semiconductor parameter analyzer controlled by a Labview program. The hardware

has a pulse-width limit of 0.5 ms in the pulse mode, but the actual output was measured by an oscilloscope to be at ~ 20 ms. The speed of individual switching events in the nanogap systems was measured by combining the Agilent 4155C semiconductor parameter analyzer with a data acquisition system (NI USB-6251 BNC) with the pulse width limit at ~ 2 μs (Chapter **2**). The switching speed at ~ 2 μs in the nanogap systems is consistent with other research employing metal nanogap structures,[76] although the switching was attributed to metal-filament switching[76,77] (more discussion of the SiO_x behavior being similar to molecular/nanomaterial systems is in Chapter **5**).

We further tested the SiO_x-switching speed limit by using an Agilent B1500 semiconductor parameter analyzer equipped with a pulse generator. The switching speed test is still based on a single switching event, that is, by outputting a pulse from the pulse generator and then shifting to the (source/monitor units) SMUs for conductance measurement, as the system is not equipped with an automatic selector between the pulse generator and the SMUs. Pulse tests were performed in both polySi-SiO_x-polySi (40 nm SiO_x) and TiW-SiO_x-TiW (40 nm SiO_x) vertical sandwiched structures, which are illustrated in Fig. 50a and Fig. 29a, respectively. As is discussed in Chapter **2**, the switching is largely electrode-material independent and is the intrinsic property of SiO_x. The TiW-SiO_x-TiW devices share the similar resistive switching features (Fig. 50) and the pulse testing result as seen in the polySi-SiO_x-polySi devices.

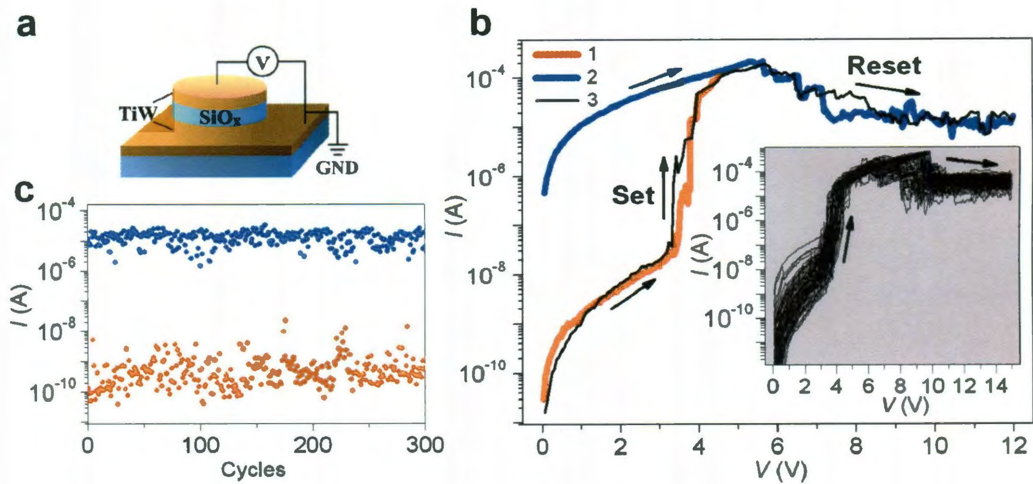


Figure 50. Electrical characterizations in E/SiO_x/E devices. (a) Schematic of the structure of E/SiO_x/E vertical cell and its electrical characterization setup. (b) *IV* curves in a formed TiW/SiO_x/TiW (120 nm/40 nm/120 nm) device. The numbers aside the curves indicate the voltage sweep order and the black arrows indicate the sweep directions. Inset shows 80 consecutive *IV* curves from a polySi/SiO_x/polySi (70 nm / 40 nm / 70 nm) vertical device. (c) Memory cycles in a TiW/SiO_x/TiW device using +5 V, + 12 V, and + 1 V as set, reset, and read voltages, respectively. The set and reset currents are not shown here.

Fig. 51 shows a series of programming pulses (top panel) and the corresponding device conductance immediately after the pulse (bottom panel, read at +1V) from a TiW-SiO_x-TiW device. It shows that: (a) the switching speed for both set and reset processes fluctuates and varies between different events; (b) a rough trend is seen that the device requires a longer set voltage pulse to program if it has been reset by a longer reset pulse; (c) the reset and set pulse-width limits are at ~ 100 ns and 50 ns,

respectively; (d) the device has various conduction states (this has also been frequently observed in device memory cycling, *e.g.*, Fig. 50c).

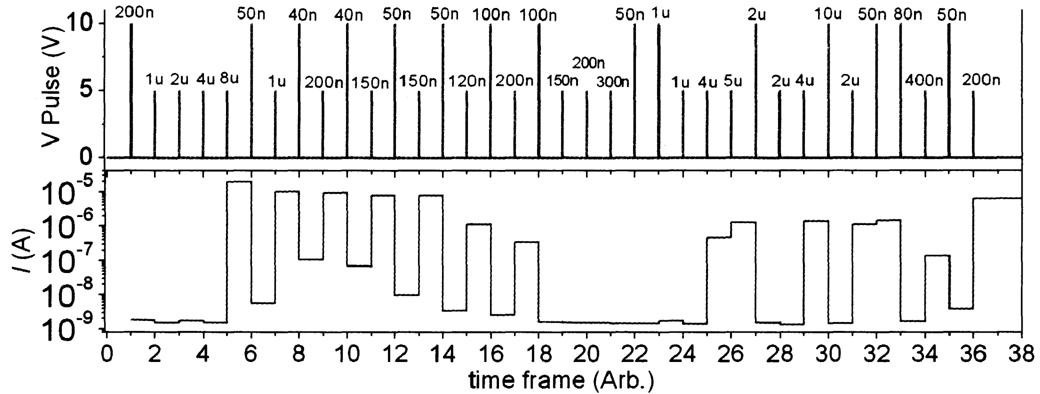


Figure 51. A series of programming pulses (top panel) and the corresponding device conductance immediately after the pulse (bottom panel, read at +1 V) from a TiW-SiO_x-TiW device.

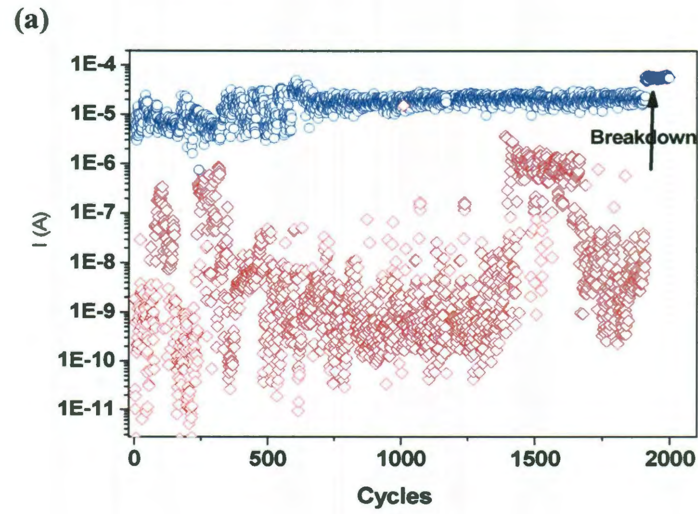
It should be noted that the input pulse width was verified by an oscilloscope in an open circuit. However, the actual pulse shape across the device during the test was not monitored. Capacitance effects could be involved that would affect the actual switching speed. The conductance fluctuation during memory cycling is an indication of (local) micro-structural morphology variations in the filament between individual programming events. And the variation in the pulse widths is another indication, for example, that a longer reset pulse may result in more micro-structural changes in the filament which therefore requires a longer set pulse to heal.

3.4-6 Memory Endurance

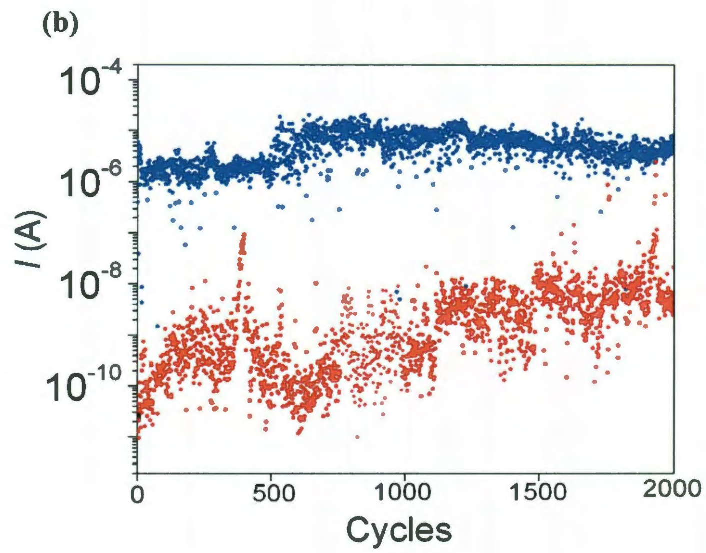
One of the main goals of the development of resistive switching memory is to serve as a potential alternative or even replacement of flash memory.[3,12] This requires a memory endurance comparable to or beyond that in flash technology (~10^4-10^6 cycles). Memory endurance of over 10^6 has been demonstrated in NiO resistive memory cells.[78] Very recently, memory endurance of 10^{10} and 10^{12} has been demonstrated in TaO_X-based resistive memory,[79,80] pushing it toward the criteria of a universal memory.[80]

As discussed previously, the memory cycling tests were performed using an Agilent 4155C semiconductor parameter analyzer. The actual output of the pulse width was measured to be ~ 20 ms (1 s period). Fig. 52a shows a typical memory cycling from a polySi-SiO_X-polySi device. It shows fluctuations in both ON and OFF states (in particular the OFF states) and that the device becomes non-switchable (hard electrical breakdown) after over 10^3 cycles. While the fluctuations and cycles can be different from device to device (Fig. 52b and Fig. 52c), they convey the similar information that micro-structural changes in the filament are involved during the programming processes and upon a certain amount of electrical stress, failure/collapse happens.

(a)



(b)



(c)

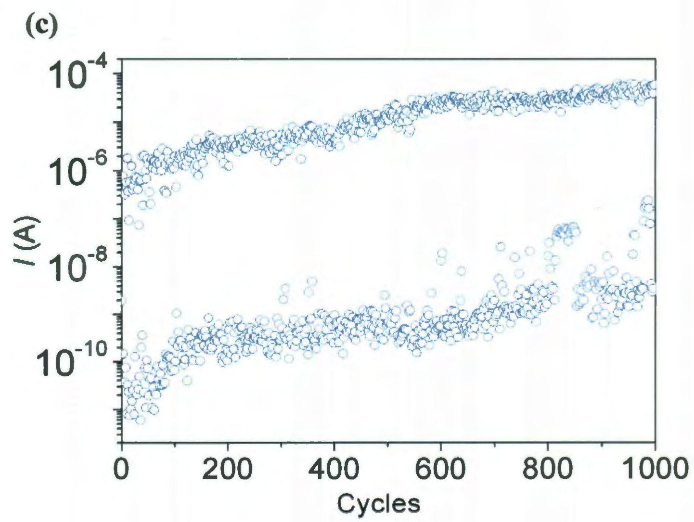


Figure 52. Memory cycles in polySi-SiO_x-polySi devices. (a) Memory cycles in a pore structure. (b) Memory cycles in a 50 μm circular polySi-SiO_x-polySi (40 nm SiO_x) pillar structure by dry-etching method. (c) Memory cycles in a 50 μm circular polySi-SiO_x-polySi (40 nm SiO_x) pillar structure by wet-etching method.

One assumption is that if the SiO_x-switching failure level is not only determined by the cycles but also related to the total electrical-stress time (the products of cycles and pulse width) hence reducing the pulse width could, in principle, prolong the memory endurance. This kind of primary test was done using the Agilent B1500 semiconductor parameter analyzer equipped with the pulse generator. However, as there was no automatic selector between the pulse generator and SMU units, the memory state after each programming pulse could not be instantly monitored. Instead, the test was performed by applying a series of programming pulses with manual switchability check between each series of programming pulses. Fig. 53 shows the testing result from a polySi-SiO_x-polySi device with ~ 10^4 cycles. While this primary data may indicate that programming pulse width could affect the endurance, further study is needed, with instant memory-state readout during the programming process.

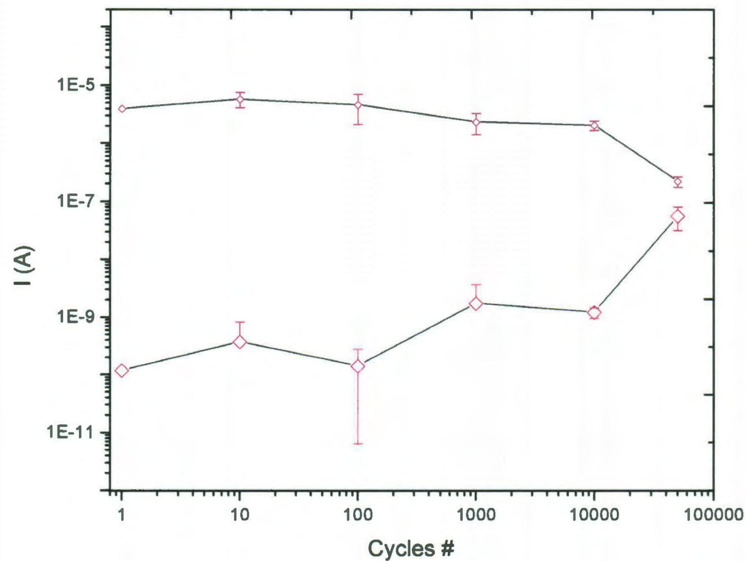


Figure 53. Memory endurance in a polySi-SiO_x-polySi devices (pulse period 10 ms, 5 μs reset pulse, 50 μs set pulse).

3.5 Summary

From metal electrodes to metal-free silicon electrodes, the intrinsic SiO_x switching picture is gradually reinforced. The fact that the current does not scale with device size indicates that the conduction and switching is through a highly localized pathway (filament). The X-ray and thermal resilience data indicate that the conductance change is not likely to be charge-based. The observed morphology change in SiO_x during the electroforming process and conductance fluctuations in memory cycling further indicate micro-structural changes during switching. In other words, the composition of the filament is different from the original SiO_x matrix and could evolve between different memory states. These indications provide the

feasibility of visualizing the filament in SiO_x and motive the mechanistic study covered in the following chapter.

It should also been noted that systematic study covering the memory performance in resistive switching memory has been rare mainly because of device variations.[12] From the mechanistic point of view, this is because the formation of the filament (electroforming process) is largely uncontrollable. An understanding of the switching mechanism can in turn help to engineer the device structure for optimal performance.

Chapter 4

Probing the Conducting Filament in SiO_x Memory Devices and Mechanistic Implications

4.1 Static TEM Imaging of the Filament

While a picture of conductance change induced by an electrical or electrochemical process is generally acknowledged in various resistive switches,[12,13] the lack of the actual visualization of the switching path,[12] particularly its material composition, adds to the debates over the mechanisms.[27] The difficulty is partially attributed to the localized nature of the switching. While nanoscale local switching is promising for device scaling,[11] the small switching volume makes it challenging to find the precise active sites.

The localized conduction and switching in SiO_x have been indicated both from the non-scaling property in the current with respect to the device size (Fig. 37f) and the localized morphology change during electroforming processes (Fig. 38). In particular, the independence of switching on electrodes in SiO_x as discussed in Chapter **2** enables the use of other materials as electrodes that could provide further constriction, since conducting filaments can be strictly confine[27,72] and require accurate positioning. Generally, a planar structure also eases the probing compared to vertical sandwiched structures as discussed in Chapter **3**. So in this chapter, we return to planar SiO_x structures and utilize the unique properties of some electrode materials to assist the locating of the filament in SiO_x. We then use transmission electron microscope to examine the switching region and identify the filament.

4.1-1 Locating and Visualizing the Filament

Carbon nanotubes (CNTs) provide the natural lateral constriction for this mechanistic investigation. As shown in Chapter **2**, by electrical breakdown, a nanogap in the CNT can be defined. The CNT-SiO_x-CNT nanogap system, with the two broken CNT ends serving as effective electrodes (Figure 54a), shows the characteristic switching (Figure 54b, c). The switching is attributed to the SiO_x at the nanogap region instead of a mechanical switch by the two broken CNT ends because: (1) forming-correlated damage to the SiO_x at the nanogap region is always observed (see Fig. 55 for a detailed forming description); (2) the switching is highly repeatable whereas mechanical CNT switches normally operate for only a few (<10) cycles;[60] (3) a CNT nanogap on a Si_3N_x substrate could not induce switching.

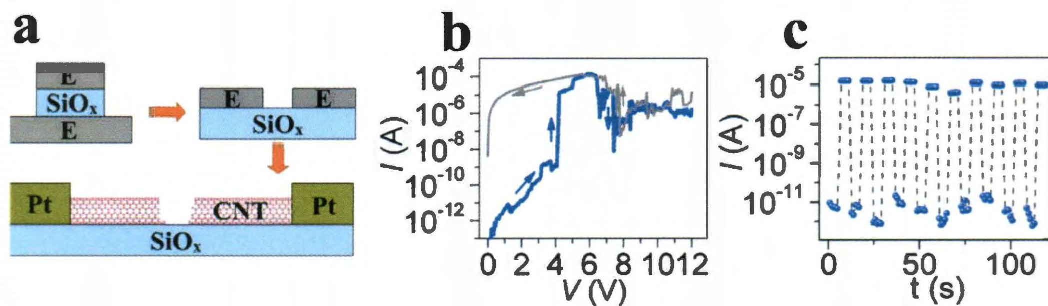


Figure 54. Switching in a CNT-SiO_x nanogap system. (a) A schematic of conceptually transferring a vertical stacking E-SiO_x-E (E denotes the conducting electrode) structure to a planar one, and then to a laterally confined embodiment by using the two broken ends of an electrically broken CNT as effective electrodes. (b) Characteristic *IV*s in a CNT-SiO_x nanogap system. (c) Switching cycles (read by +1 V pulses) in the CNT-SiO_x nanogap system with a set and reset voltage pulse of +6 V and +12 V, respectively (the programming current is not shown here).

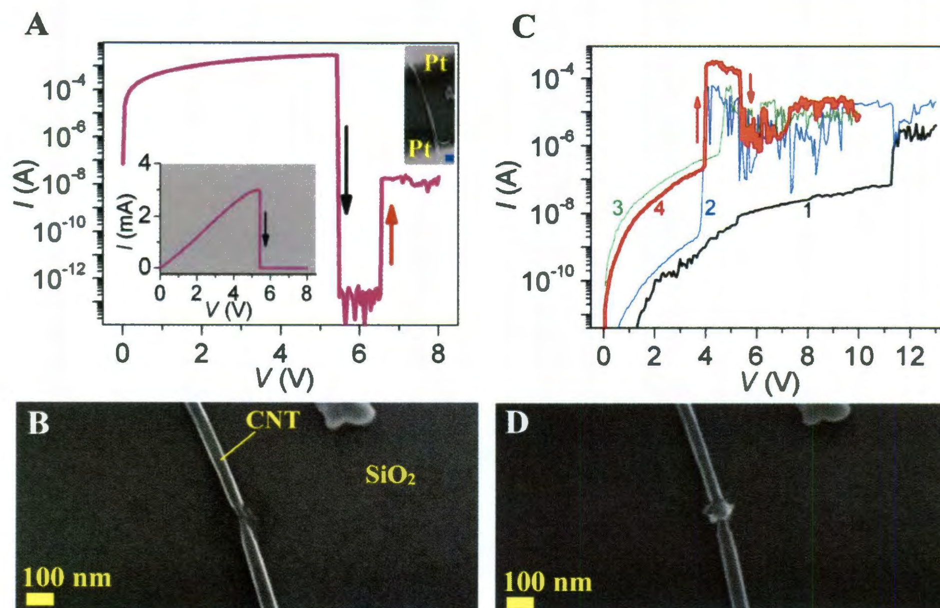


Figure 55. Formation of switching in a CNT-SiO_x nanogap system. (A) An electrical breakdown (breakdown) *IV* curve in an as-made CNT device. The top inset shows the CNT device before breakdown (scale bar is 100 nm). And the bottom inset shows the same *IV* in linear coordinates. (B) The corresponding SEM image of the CNT device after the breakdown. Before breakdown, the CNT device showed linear *IV* behavior (bottom inset in (A)). At ~ +5.5 V, a sudden current drop occurred (indicated by the black arrow in the bottom inset in (A)), indicting that electrical breakdown in the CNT was induced. The corresponding SEM image in (B) revealed that a gap region in the CNT was produced. By re-plotting the *IV* curve using a log format, more information is revealed. Immediately after the electrical breakdown in the CNT at ~ +5.5 V (indicated by the black arrow in (A)), a sudden conductance jump occurred at ~ +6.5 V (indicated by the red arrow in (A)). This conduction after the electrical breakdown in the CNT was attributed to the initialization of a forming process in SiO_x at the gap region for its low-magnitude, nonlinearity and fluctuations. In fact, this correlates well to the discernable damage to the SiO_x substrate at the gap region (shown in (B)) immediately after the electrical breakdown in the CNT, as a high local

electrical field would immediately follow after the gap generation. (C) The subsequent forming process in the CNT-SiO_x nanogap. After the formation of the nanogap, subsequent voltage sweeps (curves 1-4, with the numbers indicating the sweep order) led to the characteristic switching *IV* (red curve). (D) The corresponding SEM image of the gap region after the forming process revealed a morphology change in the SiO_x substrate (compared to that in (B)).

The confined switching site was then sliced out into a 80 nm thin piece by focused ion beam (FIB, University of Houston) and examined under TEM (JEM 2100F) (see schematic in Fig. 56). Remarkably, out of the amorphous SiO_x background, nanocrystals (NCs) at the switching site are observed (Fig. 57). NCs were only observed in the gap-region, therefore ruling out FIB-induced NC formation. For the limited elements involved here, possible crystals are only Si, graphite, and Pt (electrical wiring material to the CNT at the far ends). The measured lattice spacing in the NCs is either between 0.30 nm and 0.32 nm or at 0.19 nm, corresponding to those in Si NCs.[81] In contrast, the lattice spacing is 0.34 nm in graphite and 0.23 nm in Pt, both of which are outside of the observed range.

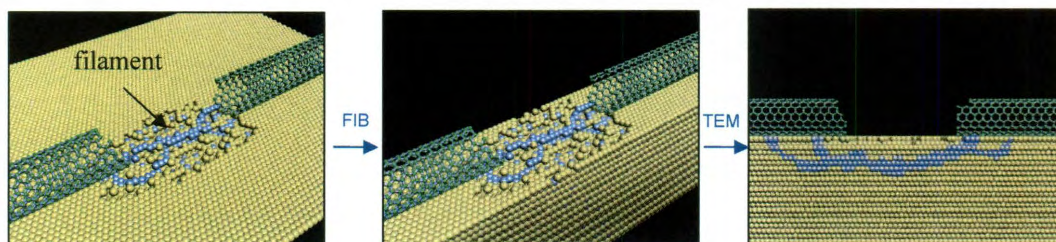


Figure 56. Schematic of cutting out the CNT-SiO_x-CNT switching sit by FIB and then

examined under TEM.

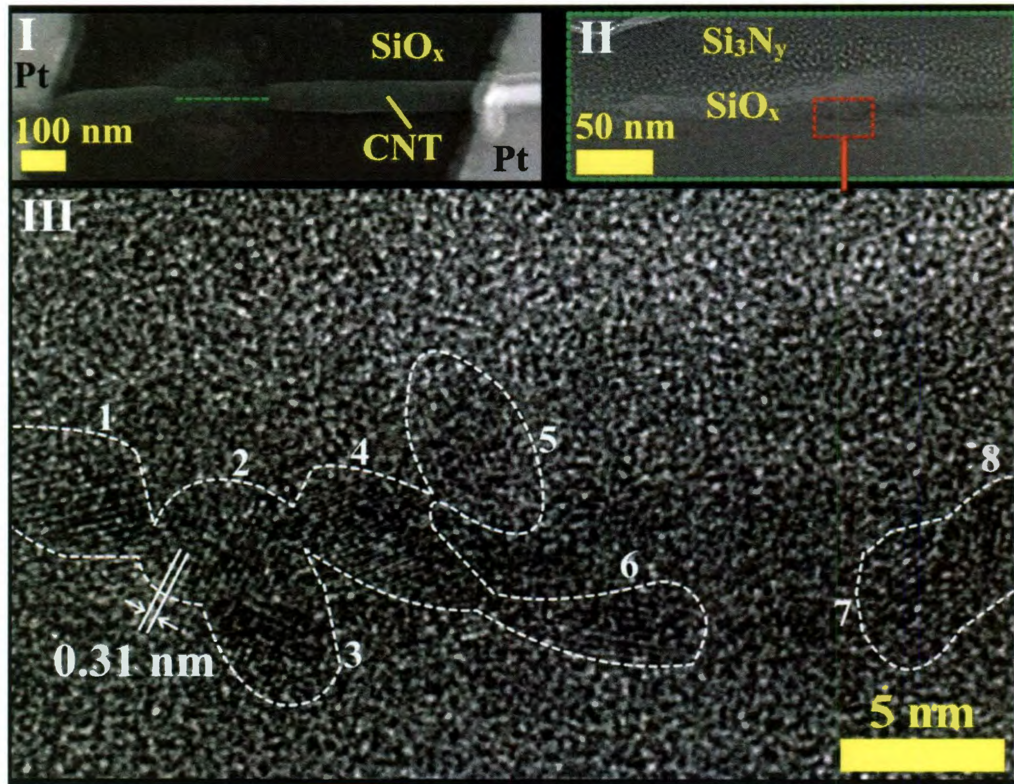


Figure 57. (I) SEM image of the switching CNT-SiO_x nanogap system. The dashed green line indicates the FIB-cut location. The device was in an OFF state before the FIB-cut. (II) The TEM image of the cross section corresponding to the dashed green line in (I). Note that an amorphous Si_3N_y layer was grown on top of the CNT-SiO_x system as a protecting means during the FIB cut. (III) A high-resolution TEM image of the region as indicated by red dashed rectangle in (II). Nanocrystalline structures are delineated by white dashed lines. The measured lattice spacing in each numbered region (from 1 to 8) is 0.30, 0.31, 0.31, 0.19, 0.32, 0.31, 0.31, and 0.32 nm, respectively. Note that the lattice spacing of 0.19 nm corresponds to that in a Si(220) plane[81] while the rest of the values are commonly attributed to that in a Si(111) plane.

The Si NCs align in a pathway that is parallel to the current flow direction (Fig. 57). We propose that this Si pathway composes the switching path or filament. This is supported by the previous test that the stored ON states survive at a temperature as high as 700 °C in Ar/H_2 environment but degrade significantly in air as a direct consequence of oxidation (Fig. 47). And the robust X-ray resilience indicates that the switching is not based on charge-trap induced conductance modulation in the Si filament. Both ON and OFF states show no obvious degradation (Figure 46) after exposure to X-ray radiation (8 KeV) at an estimated dose of 2 Mrad (SiO_2), a value more than one order of magnitude higher than the failure level of charge-based flash memory. The Si component in the filament/conduction path also offers a possible scenario why the edge-confined switching is resilient against BOE etching (Figs. 48, 49).

4.1-2 The Proposed Mechanistic Picture

We varied the thickness of the SiO_x layer, in a way to vary the length of the silicon filament, to study the effect on the electrical behaviors. Vertical devices with SiO_x layer thickness ranging from 10 nm to 200 nm were fabricated and electroformed to switching states. The threshold set voltage (V_{th}, defined as the voltage value at which the set process begins) with respect to SiO_x thickness is plotted in Fig. 58a. It shows largely thickness-independent behaviors, with the V_{th} concentrated between 3.5 and 4 V. This weak SiO_x-thickness dependence or filament-length dependence supports the mechanistic picture of point switching in the filament (see illustration in Fig. 58b): for

the large OFF resistance, the set voltage drops mainly across the broken point in the filament regardless of the filament length. The V_{th} also seems to indicate an intrinsic threshold voltage value at which some silicon conversion/transfer process begins as to heal and reconnect the broken point. It is thus likely that the set process correlates to certain electrochemical process which requires specific electrical potentials. As the only elements in the system are oxygen and silicon, we propose that an electrochemical reduction process of $SiO_y \rightarrow Si$ is involved in the set process to reconnect the silicon filament. The reset process, on the other hand, is through an oxidization process of $Si \rightarrow SiO_y$ mainly driven by current local heating for its voltage-polarity independence and higher voltage magnitude. This picture is consistent with the tunneling conduction (*i.e.*, $I \propto V^{1/2}$) in the OFF states. Furthermore, as trivial micro-structural differences at the Si bridging ends are expected between individual reset events, tunneling current fluctuations in the OFF states are expected (*e.g.*, see Fig. 50c).

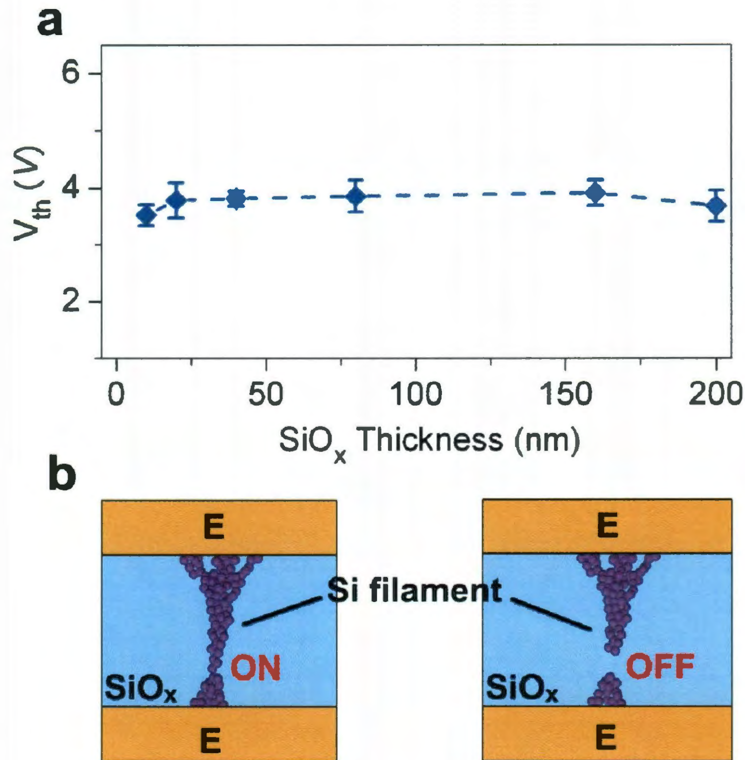


Fig. 58 (a) V_{th} from devices with different SiO_x thicknesses. Data points at 40 nm, 80 nm, 160 nm and 200 nm were collected from TiW/SiO_x/TiW structures while data points at 10 nm and 20 nm were collected from polySi/SiO_x/polySi structures. The reset voltages were at +12 V (+10 V for the 10 nm devices to avoid hard breakdown in the SiO_x layer). (b) Schematics of ON and OFF states resulting from a point switching in a silicon filament embedded in the SiO_x matrix.

With the visualization the conduction path (Fig. 57), we can do an estimation of the switching speed based on the mechanism we proposed. Suppose that during a set process, a region of d ~ 5 nm involves the reduction process $SiO_x \rightarrow Si$ to re-bridge the Si path. Consider a spherical SiO_x (x ~ 2) region with d ~ 5 nm, the number of

charges required to reduce Si^{4+} to Si is $N = \frac{4}{3}\pi(d/2)^3 \cdot \rho \cdot \frac{N_A}{M} \cdot 4$, where ρ, M, N_A are the density of SiO_x, molar mass of SiO_x, and the Avogadro constant, respectively. So the minimum switching time is $\Delta t = Ne/I$, where e, I are the electron charge and OFF current at the set voltage, respectively. Based on the *IV* sweep (blue curve in Fig. 54b), the OFF current I at the set voltage (+ 6V) can be obtained by extrapolation using $I \propto V^{1/2}$, and is estimated to be ~ 2×10^{-8} A. So the calculated Δt is ~ 40 ns. This estimation is close to the actual switching speed achieved in the devices (*e.g.*, ~ 100 ns in the set process, see Fig. 51). This picture is further supported by the fact that a set process cannot be performed in air (Fig. 42) but can be done in nitrogen or vacuum (10^{-5} Torr), as oxygen environment hinders the reduction. As both Si and SiO_x are stable materials, the switch shows robust nonvolatile properties with an extrapolated retention time beyond 10 years (Fig. 41).

The above proposed electrochemical redox process can also account for the multi-level states (Fig. 22b) and corresponding V_{th} shifts observed in the SiO_x devices. In the same device, a lower magnitude in the reset voltage usually results in an increased OFF conductance and it also slightly shifts the V_{th} to a lower magnitude (see Fig. 59a, or in Fig. 22a). The conductance modulation in the OFF states by different reset values enables the possibility of multi-bit memory. Meanwhile, the device-size independence in the ON states indicates that this conductance modulation is through single or few filaments, not a collective effect from a large number of filaments. In other words, it is the structural/compositional variation at the switching

point in the filament that governs the conductance modulation. In the mechanistic picture that a reset process is through Si → $SiO_{y,}$, it is expected that the final valence state of the Si^{2y+} in SiO_y will affect the conduction. More generally, higher valence state in Si^{2y+} (or richer oxygen concentration) is likely to result in a more insulating state (Fig. 59b). A higher magnitude in the reset voltage should result in a more complete oxidization process and hence lower conductance. On the other hand, for the electrochemical process of SiO_y → Si involved in a set process, the lower the valence state in the Si^{2y+} the less energy or electrical potential (applied voltage) is required for the reduction. Therefore, a decrease in the magnitude of the reset voltage results in the shift of V_{th} toward a lower magnitude as well. Note that valence states of Si^0, Si^+, Si^{2+}, Si^{3+}, and Si^{4+} were indeed observed and identified in SiO_x and the binding energy increases as the valence state increases.[82]

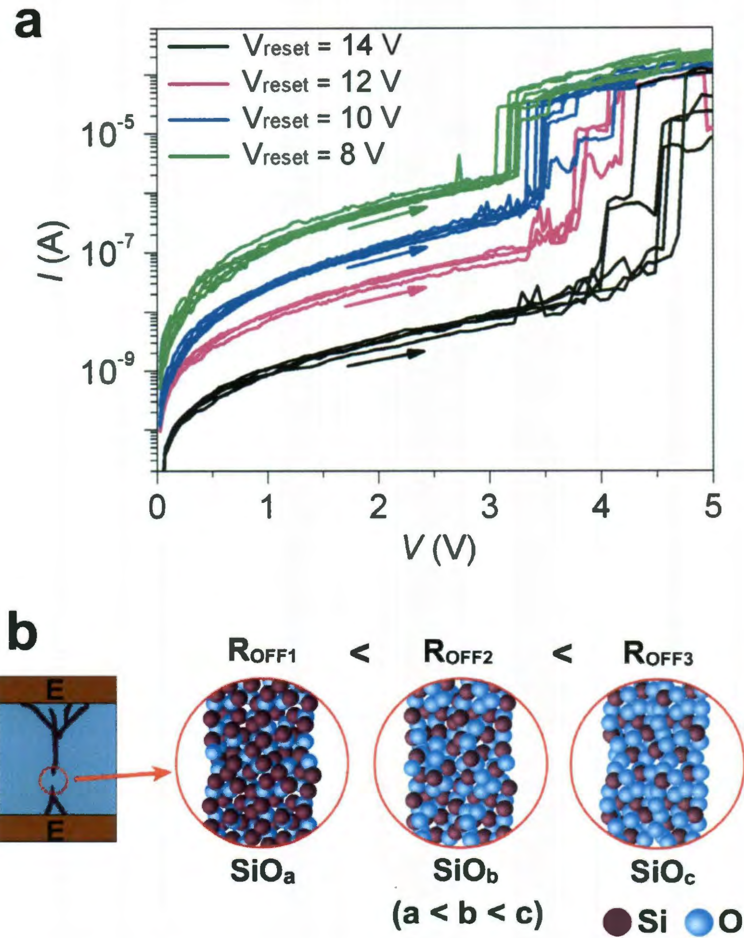


Figure 59 (a) *IV* curves of the set processes in a same TiW/SiO_x/TiW (40 nm SiO_x) device. Each set *IV* curve was obtained after a reset process, with different colors indicating different reset voltage values. The black, magenta, blue, and green colors correspond to set *IV* curves after +8 V, +10 V, +12 V, and +14 V reset operations, respectively. (b) Schematics of the valence states of silicon (or oxygen concentrations) at the switching site in the filament with respect to different OFF conduction states.

The CNT electrodes ensure that the only source for the formation of Si NCs is SiO_x. This is consistent with the electrode-independent switching in SiO_x. As the forming process can induce local crystalline structural changes, it is possible here that

the forming process breaks the Si-O bonds to form direct Si-Si bonds, which then aggregate into NCs. Another similar scenario is to consider the movements of oxygen vacancies[83] as the cause of the local material composition change. The forming process is found to be not only field-driven but also thermal-related. A substantial current level (10^{-6} A) needs to be reached before a forming process takes place; otherwise a hard breakdown (non-switchable high-conductance state) is more likely to happen. This indicates that local current heating is also necessary, as heat is found to help Si aggregation in SiO_x.[84] Consequently, a forming process could not be initialized at temperatures below 150 K in our experiments. The forming process is more readily induced at the surface of the SiO_x, as surfaces are more defective and thus more subject to leakage. Thermal annealing tends to introduce more defects at the surface thus assisting the forming process. Therefore, the switching is not intrinsically surface-confined. While a smaller x value in the SiO_x could result in an easier electroforming process, the Si-pathway picture suggests that once the NCs are formed, the switching is less likely to be x-dependent. The Si-pathway picture provides guidance into engineering SiO_x (*e.g.*, through local Si doping) to make resistive switches for memory and logic applications.

4.2 *in situ* Imaging of the Filament

4.2-1 Challenge and Opportunity

The visualization of the silicon filament discussed above provides more insight

into the intrinsic switching properties of SiO_x. Similar techniques combining FIB and TEM were used in other resistive memory system for the study of the composition of the filament.[72] While it is difficult to locate the actual functional filament region for multi-filament switching systems,[72] utilization of the CNT electrode provide a method to localize the filament (Section **4.4-1**). Nevertheless, FIB-cut imaging is destructive in that one needs to destroy a working device in order to image the functional region. Other arguments could be rendered with respect to the formation of the filament, as high-energy ion beam used in the sample-preparation stage of FIB might induce micro-structural changes within the sample itself. Therefore, *in situ* imaging of the filament formation is essential for the further investigation of the mechanism. Moreover, for the point-switching scenario as discussed above, it is also possible to visualize the dynamics of the filament during the switching event, providing more details into the mechanism.

To date, *in situ* imaging of the switching dynamics in resistive switching systems has been rare.[12] The difficulty lies not only in the dearth of *in situ* nanoscopic instrumentation but also the strict design of an effective nanostructure for probing. Since Rice University does not have the capability of *in situ* electrical characterization in the TEM system, a TEM holder that is capable of electrical signal input was designed and fabricated (Fig. 60, also see Appendix for details).

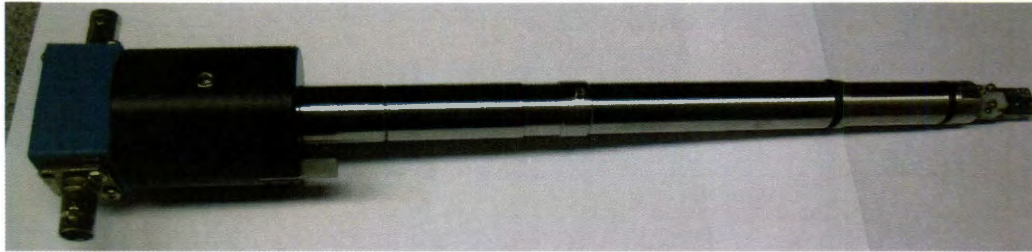


Figure 60. TEM holder (for JEM 2100F TEM system) that is capable of *in situ* two-terminal electrical characterization.

4.2-2 Device Design and Fabrication

Figs. 61a-c shows the schematics of the device design and setup for the *in situ* imaging. The imaging region consists of a SiO_x thin-walled structure covered by a layer of amorphous carbon (α-C), which is connected to external electrical inputs (Fig. 61a). By electrical breakdown in the α-C layer, a disruption region or nanogap can be produced as we described previously in planar carbon-coated SiO_x devices.[52] The broken ends of α-C layer then serve as the electrodes for the SiO_x in the nanogap region. The use of α-C as the electrode material eliminates possible extrinsic effects from metals, and the electrical breakdown-generated nanogap provides an easy method for the fabrication of closely spaced electrodes atop a thin-walled structure. The confinement from the nanogap pre-localizes the switching site so that it can be constantly monitored from before the electroforming or filament formation and throughout the experiment. During imaging, the electron beam from the TEM system travels perpendicularly across the SiO_x thin-walled structure. In this configuration, the SiO_x and the α-C layer are spatially separated in the imaging plane, minimizing

possible interference from the electrode material. Practically, for the successful passage of the electron beam across the nanogap region, a multi-stage design with the SiO_x thin-walled structure is required (Fig. 61b). This multi-stage device is then vertically mounted on a home-built TEM stage (Fig. 60) that is capable of *in situ* electrical characterization (Fig. 61c).

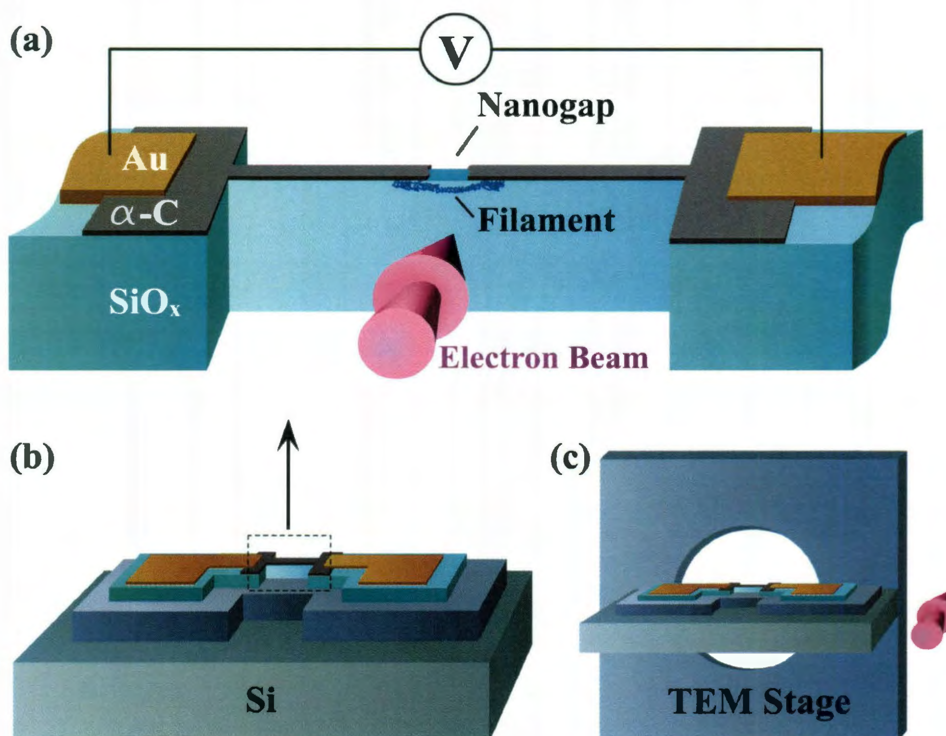


Figure 61. (a) Schematic of the SiO_x thin-walled structure for *in situ* TEM imaging. The switching region in SiO_x is localized by the nanogap generated in the α-C layer and imaged by TEM. (b and c) Schematics of the multi-stage structure and its arrangement with respect to the TEM stage. The pink arrows indicate the TEM electron beam imaging direction.

The multi-stage SiO_x thin-wall structure as shown in schematic in Fig. 61 is

fabricated from a silicon wafer (thickness ~ 500 μm) capped with 2 μm thermal SiO_x (x ~ 2) on top. It includes the following steps Fig. 62:

1. Cr sacrificial mask (~ 400 nm thick) is defined by photolithography. Reactive ion etching (RIE) is then used to define the Si stage as shown in Fig. 63b. The etching depth for the Si stage is ~ 12 μm. CHF_3/O_2 and $SF_6/Ar/O_2$ recipes are used for SiO_x and Si etching, respectively. The Cr mask is then removed by Cr etchant (CEP-200).

2. At 900 °C, a layer of α-C is grown on top of the defined Si stage by chemical vapor deposition (CVD) method using C_2H_2/H_2 (50/150 sccm).[49] The α-C layer is ~ 20 nm thick with its resistivity ~5-6 KΩ/□. Note that low resistivity is desirable so that the resistance of the α-C electrode is comparatively lower than that of the ON state in SiO_x.

3. RIE (O_2) is performed for selected-area removal of the α-C layer, with photoresist (S1813) as sacrificial mask defined by photolithography.

4. Electrodes (Ti/Au = 5/50 nm, for wire bonding) is then defined by photolithography. Note the selected-area removal of α-C layer in step 3 is to ensure a direct SiO_x/Ti/Au contact for good adhesion during wire bonding.

5. Pt wires that connect the α-C layer and the Au electrodes are defined by electron-beam lithography (EBL). The two Pt wires are separated by ~ 3 μm atop the α-C region.

6. Narrow Cr stripe (~ 140 nm wide, 50 nm thick) between the Pt wires atop the α-C layer is defined by EBL. It serves as the sacrificial mask for SiO_x etching during the definition of the thin-wall SiO_x structure as shown in Fig. 63c.

7. A second Cr mask (~40 nm) is defined by photolithography to protect the Au electrodes during SiO_x etching. Note the Pt wires need no protection as they are resilient to the SiO_x-etching recipe.

8. RIE is used to define the SiO_x thin-wall structure with a height of ~ 500 nm (Fig. 63c). Because of undercut, the 140 nm-wide Cr mask eventually results in the width of the SiO_x thin-wall structure ~ 100 nm (top panel in Fig. 64). And the Cr mask is then removed.

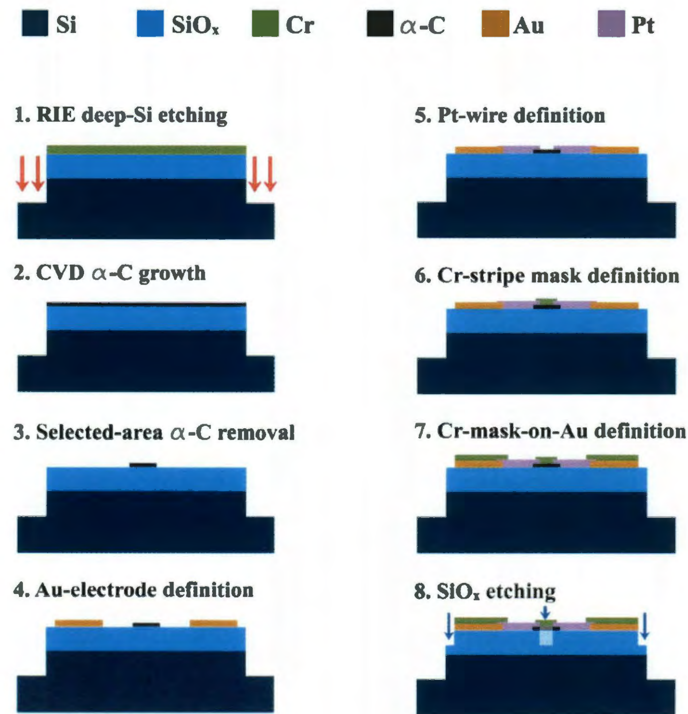


Figure 62. Fabrication flow of the device for the *in situ* TEM imaging device.

The fabricated structure above is then sliced into slim piece (350 μm ×3 mm, Fig. 63a) by a dicing saw. With the height of the SiO_x thin-wall structure ~ 500 nm (Fig. 63c), the width and height of the Si stage ~ 20 μm and 10 μm, respectively (Fig. 63b), the width of the device ~ 300 μm, the fabricated device is expected to have an angle-mismatch tolerance of ~ 0.5 degree for the electron beam. The sliced device is then vertically mounted on a home-built TEM stage (Fig. 60) that is capable of electrical input, and electrically connected through wire bonding. An Agilent B1500 semiconductor parameter analyzer is used for the electrical characterizations. The imaging is carried out on a JEM-2100F TEM system with the beam energy at 200 KeV.

Fig. 63a-c show a series of SEM images of the actual device for the *in situ* TEM imaging. Fig. 64 (bottom panel) shows a C-SiO_x thin-wall structure successfully imaged under TEM (low-resolution mode). The device parameters are specified in the caption in Fig. 63.

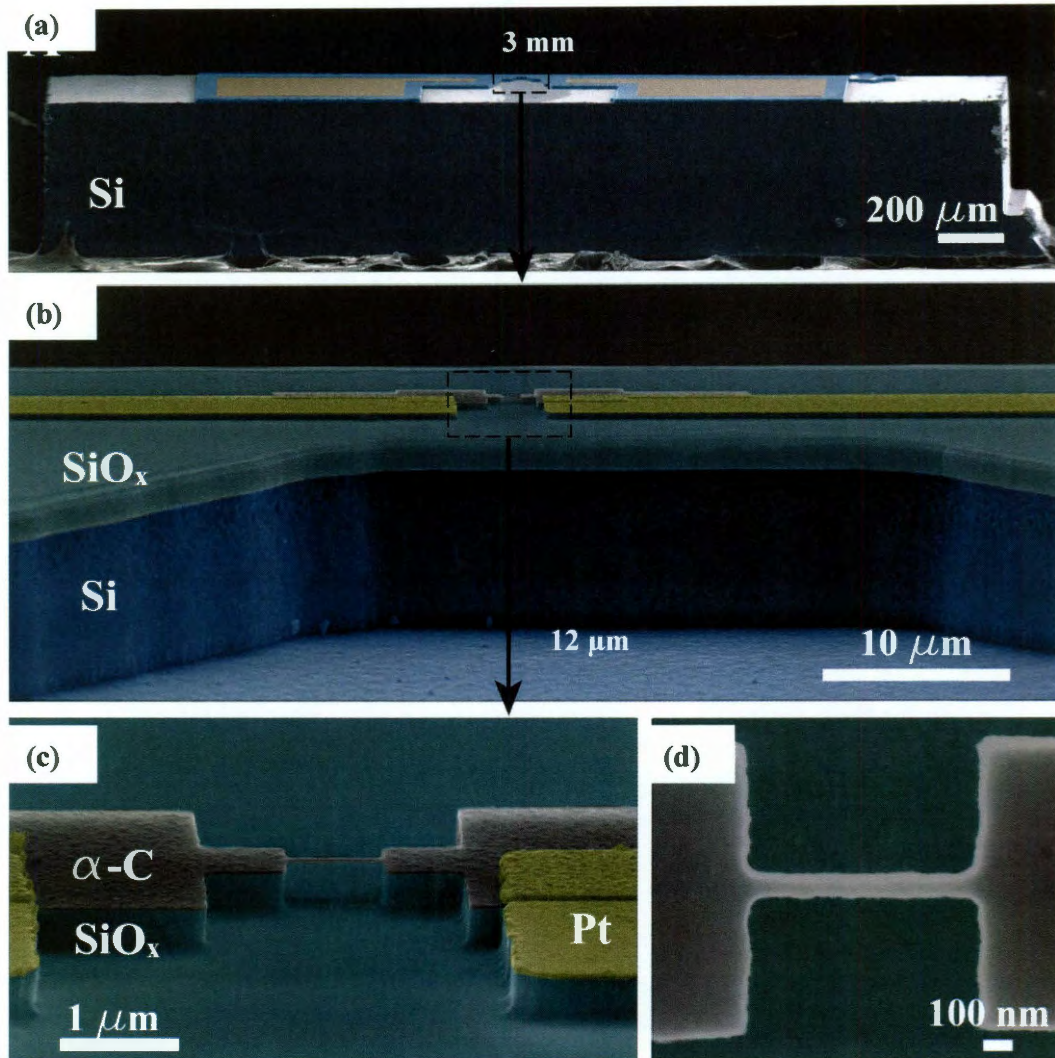


Figure 63. (a) A macro-scale Si chip (made from Si wafer with 2 μm SiO_2 on top) defined by a dicing saw (L×W×H ~ 3 mm×0.4 mm×0.5 mm). (b) On the macro-scale Si chip sits the first stage defined by deep-Si etching method. The width of the constriction region is ~ 20 μm. The height of this stage is between 10 ~ 15 μm. The electrode pad area is between ~ 200 × 500 μm^2 for wire bonding. (c) On the constriction of the first stage is the C-SiO_x thin-wall structure (electrically wired to the electrode pad for wire bonding). The C-layer thickness is 10-30 nm. The C-SiO_x thin-wall structure is ~700 nm×100 nm×350 nm (L×W×H). With these parameters, an angle tolerance of ~ 0.5° is achieved.

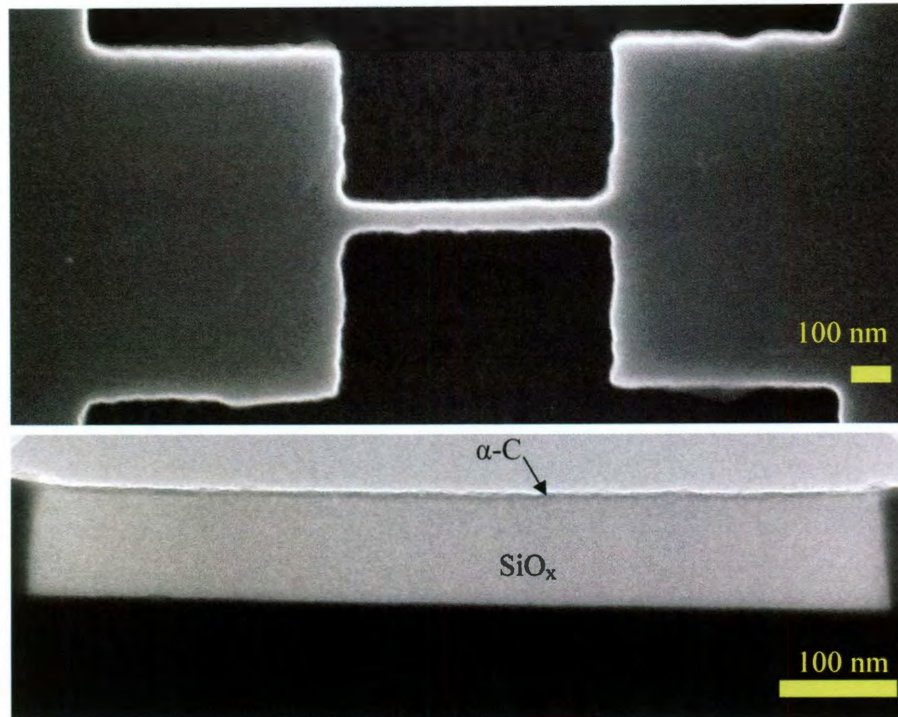


Figure 64. A top-view SEM image of a C-SiO_x thin-wall structure (top panel) and a TEM image (low-magnification mode) of a C-SiO_x thin-wall structure (bottom panel).

4.2-3 *in situ* Imaging

Fig. 65a,b show two examples of the electrical breakdown in the α-C layers in the TEM system to produce nanogaps in the C-SiO_x thin-wall structure. Upon sweeping to > 10 V, a sudden conductance decrease is incurred (middle panels). Simultaneously, a disruption in the α-C layer on top of the thin SiO_x wall is observed (bottom panels). The SiO_x layer at the nanogap region usually also becomes dented, likely because of the combined effects of current local heating and high electric field.

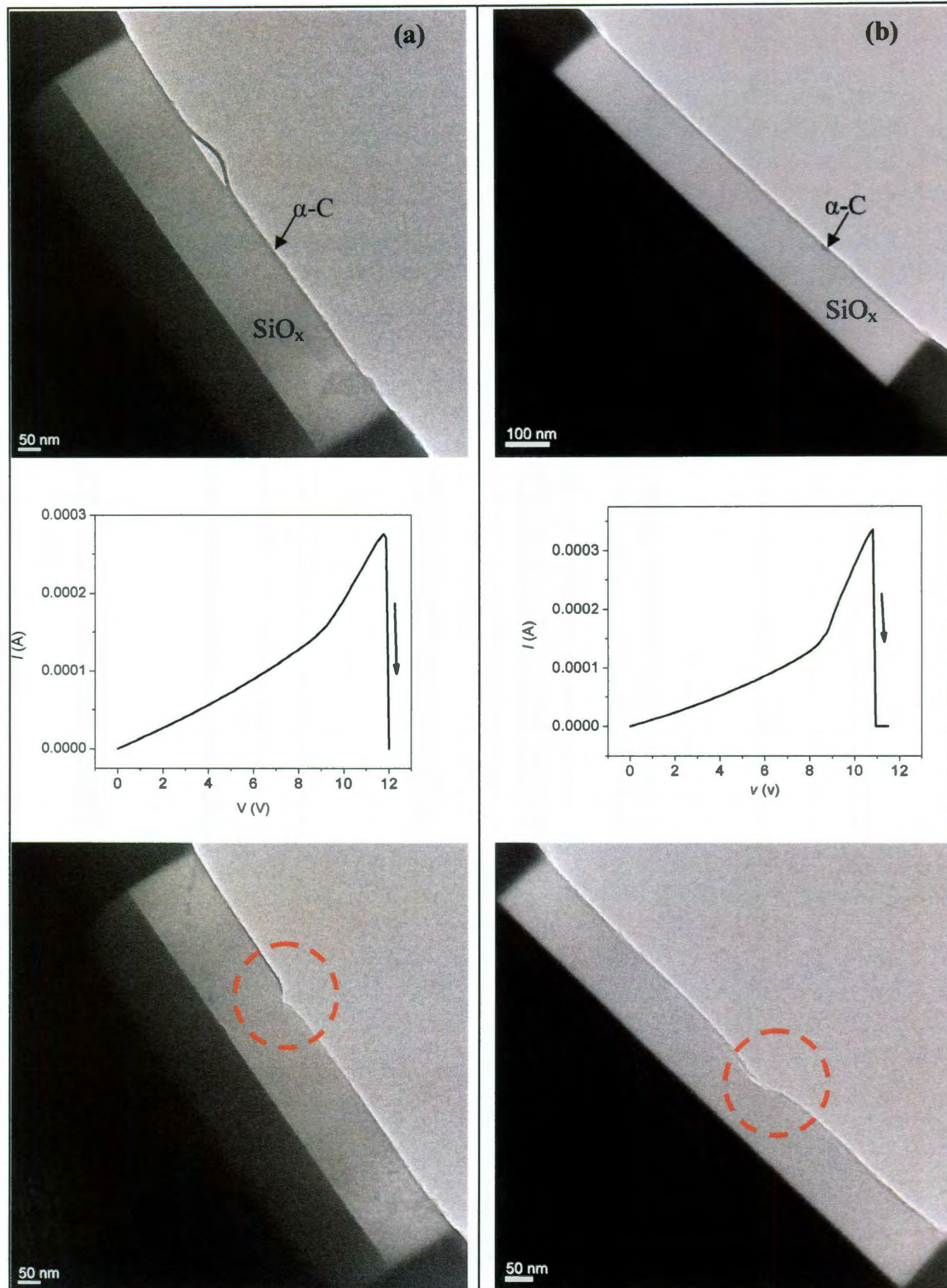


Figure 65. Top panels: two as-made C-SiO_x thin-wall structures under TEM. Middle panels: electrical breakdowns of the α-C layers by voltage sweeps to certain values. Bottom panels: disrupted nanogaps (indicated by dashed circles) after the electrical breakdowns in the α-C layers.

We found that the high-energy electron beam from the TEM system (200 KeV) impacts the SiO_x switching properties at the high-resolution mode. Specifically, the electron beam tends to not only degrade the memory state (*e.g.* the ON state), but also the switchability. As shown in Fig. 66a, with the electron beam blocked, the C-SiO_x thin-wall nanogap system showed the characteristic switching *IV* curve (blue curve). The device was then set into ON state (magenta & red curves). When the electron beam was under normal high-resolution imaging mode, magnification ~ 200 K, the ON state degraded (red curve in Fig. 66b). Moreover, the device was de-activated into a non-switchable low-conductance state (black curves in Fig. 66b). With the electron beam blocked after this several-min exposure, a re-electroforming process followed (black curves in Fig. 66c) and activated the device into its normal switching state (blue curves in Fig. 66c). This kind of phenomena can be repeated in the same device and other devices, further confirming the destructive role of the electron beam to the switching device. A shorter electron exposure time usually results in an easier (*e.g.* less voltage sweeps) re-electroforming process. The mechanistic implication of the beam impact will be discussed later.

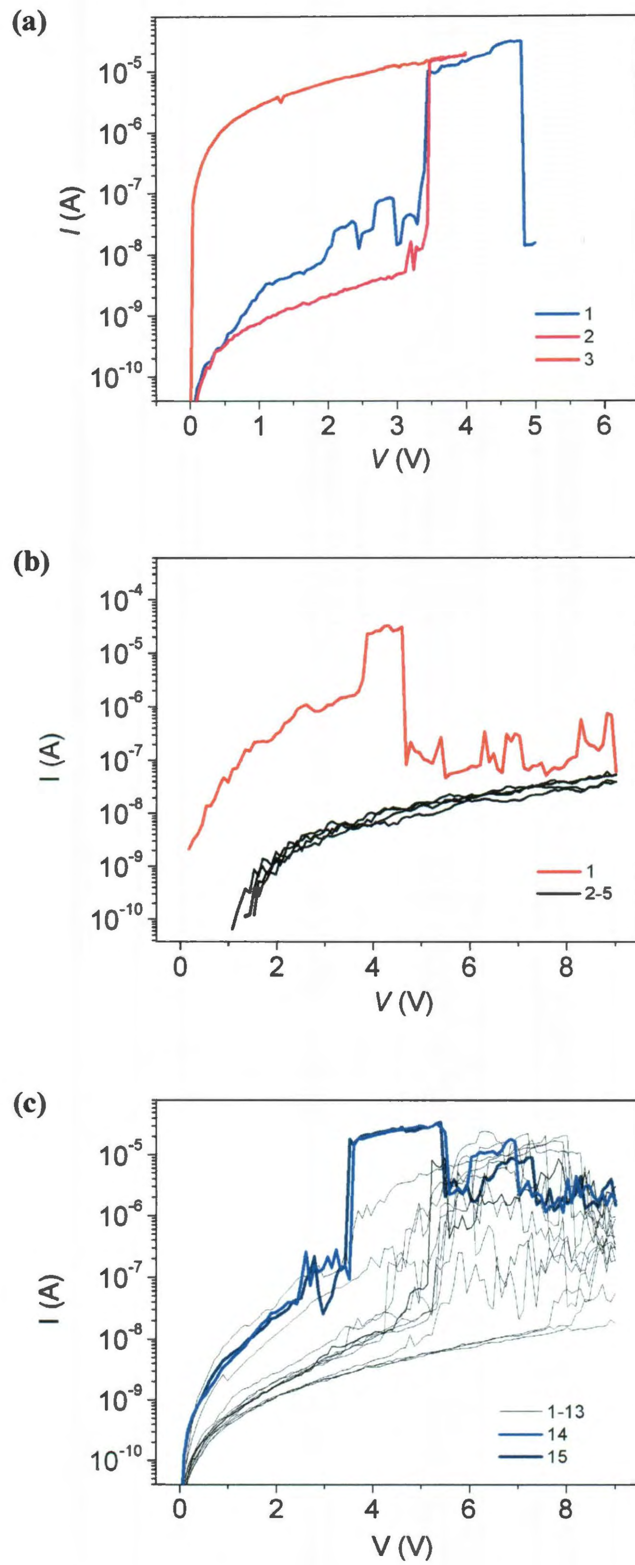


Figure 66. (a) Switching *IV* curves in a formed C-SiO_x thin-wall device with the electron beam from the TEM system blocked. The device was switched to ON

(magenta curve) and kept in the ON state (red curve). (b) When exposed to the electron beam, the ON state degraded (red curve) and no switching *IV* curves were observed with further forming attempts (black curves). (c) When the electron beam was blocked again, a re-forming process (black curves) in the device was initialized and finally the device went back into the switching state (blue curves). The numbers in the figures indicate the voltage-sweep orders.

Fig. 67 shows a series of high-resolution TEM images of the nanogap region (right panels) with respect to different *I-V* responses (left panels). Note that during the electrical characterization, the electron beam was temporally blocked to exclude beam impact as discussed above. Immediately after the electrical breakdown in the α-C layer, a nanogap of ~ 15 nm is formed (Fig. 67a). Both the SiO_x at the nanogap region and the SiO_x far from the nanogap show amorphous silica features. Because of the disruption in the α-C layer, the device shows little conduction during the subsequent voltage sweep, until at ~ 12 V the current suddenly increases (light grey curve in the plot of Fig. 67b). This conductance increase features the beginning of the electroforming process in SiO_x.[69] The device is subsequently electroformed, showing the characteristic *I-V* curve featuring current increase (at ~ 5 V) and decrease (at ~ 10 V) that define the typical set and reset processes, respectively (grey curve). The device is set to the ON state (red curve). The immediate TEM imaging shows morphological changes at the nanogap region (Fig. 67b), as is often associated with the electroforming process.[12,69] Specifically, out of the amorphous background, ~ 3 nm regions of nanocrystalline structure (based on the appearance of lattice fringes)

appear at the nanogap (bounded region and inset in Fig. 67b). The apparent lattice spacing of the nanocrystal based on the fringes is distinct from that of the α-C, indicating a different material form.

Due to the beam impact as shown above (also see discussion below), the formed ON and switching states degrade after imaging (light grey curve in Fig. 67d). A subsequent re-electroforming process is involved to set the device back to ON (grey and red curves). The immediate imaging shows growth in the nanocrystal (bounded region and inset in Fig. 67c). The partially degraded ON state after this imaging is compensated by a set process (red curve in Fig. 67d). For the subsequent voltage sweep to 14 V, a sudden decrease in the conductance occurs at ~ 12 V, featuring the typical reset process.[69] The immediate imaging shows prominent shrinkage in the size of the nanocrystal (bounded region and inset in Fig. 67d).

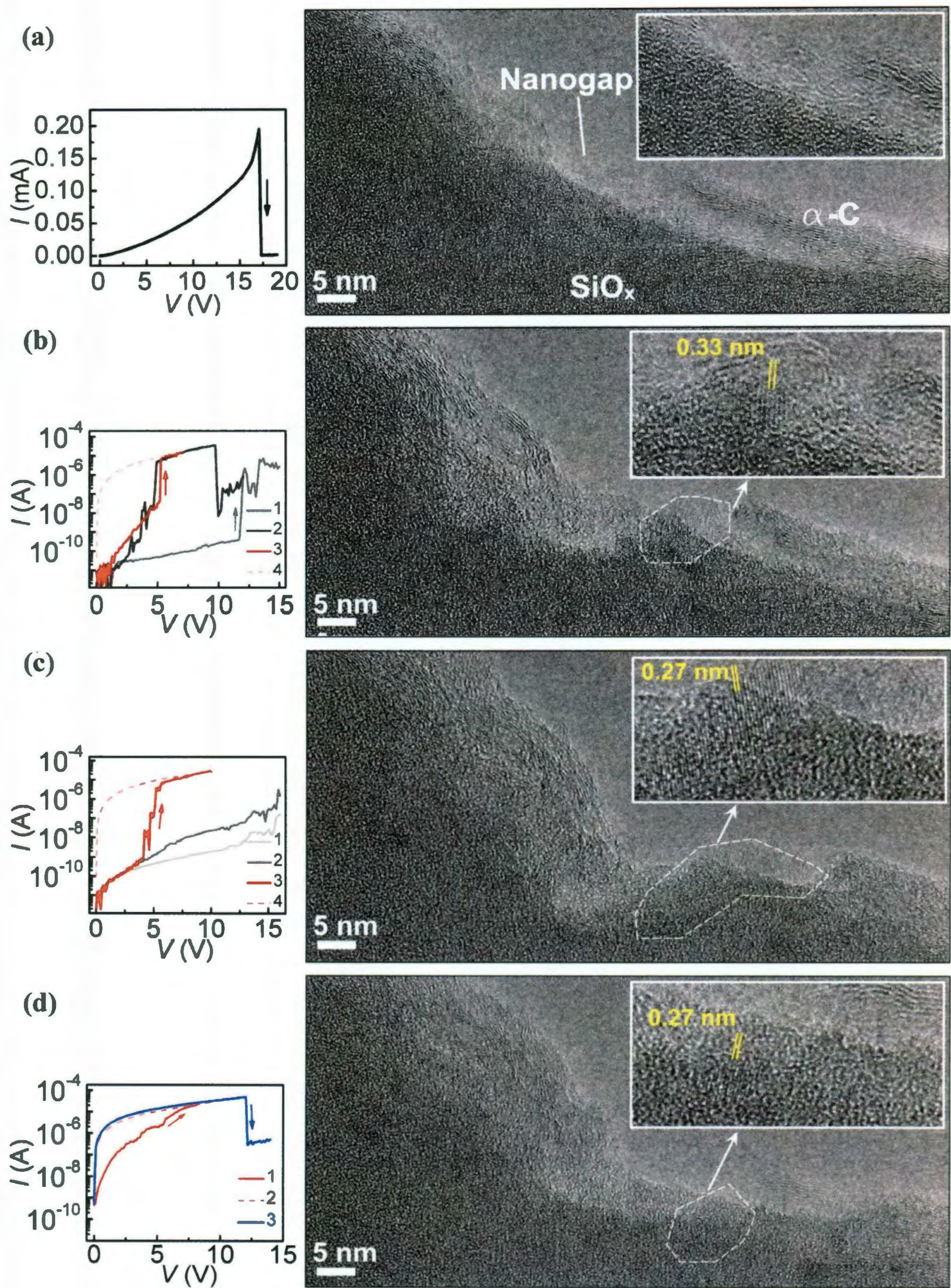


Figure 67. High-resolution TEM images of the nanogap region (right panels) taken immediately after the electrical characterizations (left panels). (a) The electrical breakdown *I-V* curve in the α-C layer and the formed nanogap. The inset shows the enlarged nanogap region which shows only amorphous features. (b) The electroforming process in SiO_x with the state set to ON. The inset is an enlarged image of the circled region, showing nanocrystalline features. (c) A re-electroforming

process in SiO_x after the imaging in (b), with the state set to ON. The inset shows the enlarged image of the circled region, showing the growth of the nanocrystal. (d) A reset process after the imaging performed in (c). The inset shows the enlarged image of the circled region, showing the shrinkage of size in the nanocrystal. The numbers in all the left-panel plots indicate the voltage-sweep orders.

The nanocrystalline structures were persistently observed only at the nanogap region in the switching devices, indicating their correlation with the electroforming and switching processes. Selected area electron diffraction shows that the crystalline structures are consistent with Si nanocrystals (NCs) and not silicon carbide. As shown in Fig. 68b, the lattice spacing of 0.27 nm and 0.16 nm and 0.14 nm can be assigned to Si-I (200), (311) and (400) planes, respectively. However, (200) plane is the forbidden plane for diffraction in diamond cubic structure.[85] Instead, it is more reasonable to assign the strong signal at 0.27 nm^{-1} to Si-III/Si-XII phases.[86] The lattice spacing of 0.27 nm and 0.16 nm and 0.14 nm correspond to Si-III (211), (400) and (422) planes.[87] More evidence is shown in Fig. 69 below. In additional, the diffraction pattern here is different from those in the SiC forms[87-89] and crystalline silica[87], ruling out the possibility of all those forms.

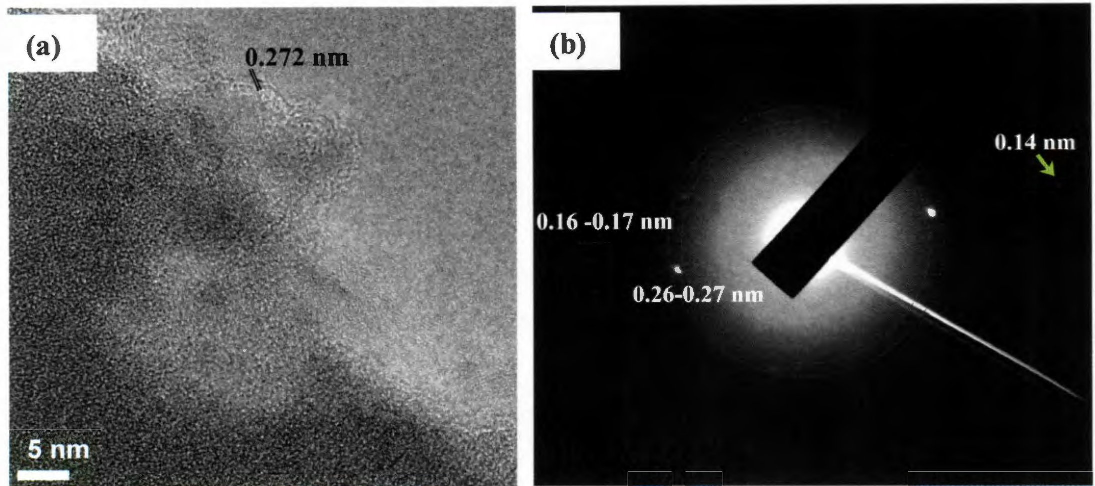


Figure 68. (a) High-resolution TEM image of a second switching nanogap (the first is shown in Fig. 67) showing the corresponding selected-area diffraction pattern for the device.

As SiO_x is the only source containing the Si element, the formation of the Si NCs shows that the energetically viable $SiO_x \rightarrow Si$ process is associated with the electroforming process. The *in situ* recording of this process also excludes the possibility of processing-induced formation during the filament isolation as was involved in *ex situ* imaging.

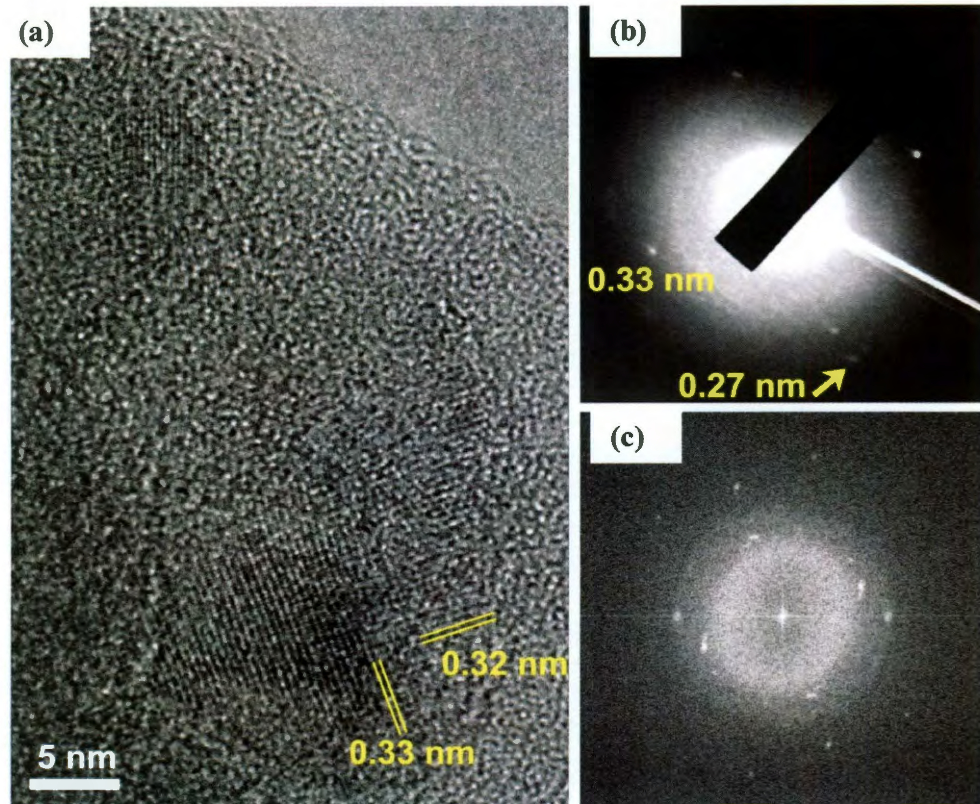


Figure 69. TEM and diffraction patterns from a different device than that shown in Fig. 3. (a) High-resolution TEM image of the nanogap region from another SiO_x switching device. (b) Selected-area diffraction pattern of the region shown in (a). (c) A fast Fourier transformed micrograph of the image shown in (a).

As the ON state shows largely metallic conduction,[25] questions arise regarding the composition of the conductor since conventional silicon is semiconducting. Lattice-spacing measurements and electron diffraction patterns from the Si NCs show evidence of structural deviation from the conventional diamond cubic Si-I phase. As shown in Fig. 69, the intersected lattice spacing of 0.33 and 0.32 nm with a nearly perpendicular angle is the feature of the Si-III phase,[86] which is semi-metallic[90] and often associated with other conducting phases.[91] This indication can also be seen in

Fig. 67; while the lattice spacing of 0.27 nm can be assigned to Si-I(200), Si-III(211) or Si-XII(11-2) faces, that of 0.33 nm (Fig. 67b) can only be associated with Si-III/Si-XII phases.[86] In particular, as Si-I(200) is the forbidden plane for diffraction,[85] the strong signal of 0.27 nm^{-1} in the diffraction patterns is further indication of the conducting Si-III/Si-XII phases[92] (Figs. 68 and 70). While these phase transitions in Si are typically induced by pressurization,[91] here it is possible that the high electric field attained at the nanogap is inducing these phases. The stability of the formed silicon phases at ambient environment[91] also accounts for the electronically nonvolatile property in SiO_x resistive switching memory. Remarkably, the suppression of the electroforming and switching in SiO_x at low temperature[25,69] coincides with the fact that the Si-III phase cannot be formed at liquid-nitrogen temperature.[93] Furthermore, the semi-metallic NCs suggest a rationale for failure to induce gating in three-terminal embodiments of these devices,[49] which was originally proposed to be carbon switching[49] and later clarified as SiO_x-derived switching.[52,69] Note that ion milling was reported to induce phase transition of Si (III/XII) → Si-I + α-Si,[93] which accounts for the possible appearance of Si-I phase in *ex situ* imaging by FIB cut shown in Fig. 57.

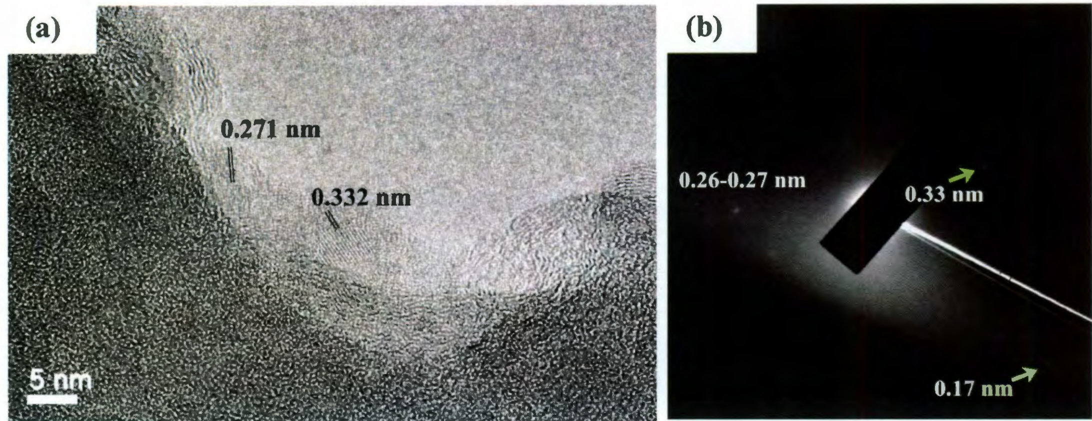


Figure 70. (a) High-resolution TEM image of a fourth switching nanogap and (b) the corresponding selected-area diffraction pattern. The diffraction pattern here shows similar feature as that in Fig. 68(b). The signal at 0.33 nm^{-1} can only be assigned to Si-III (211) or its closely-related phase Si-XII (11-1).[86] This lattice spacing along with the absence of 0.31 nm^{-1} signal (corresponding to Si-I(111)) further indicates the Si-III/Si-XII phases.

From the devices studied, the filament in SiO_x is not in the form of a continuous single crystal across the nanogap, as seen in TiO_x switching systems.[72] Instead, discrete Si NCs form across the nanogap. This feature indicates a possible transition region between the Si NCs that could favor the switching process. The growth of the Si NCs (Fig. 67c) indicates the general Si-rich nature along the nanogap in the electroformed device. This Si enrichment is also evidently correlated with the indention and shrinkage of the volume at the nanogap region, likely a result of oxygen outgassing.[71] The shrinkage of the Si NCs with respect to the conductance drop (Fig. 67d) indicates the possible amorphization process. This is consistent with the

thermally induced amorphization observed in the metallic Si phases,[91,92] as the reset process in unipolar resistive switching is largely thermally driven.[69] In particular, resistance increase is associated with the amorphization process.[93] This provides a possible scenario for the filament rupture in the reset process.

We further take the electron-beam impact into consideration during the mechanistic interpretations. As mentioned above, the electron beam from the TEM system tends to degrade the conduction and switching state in SiO_x. This does not indicate a charge-based mechanism though, as that was ruled out in the x-ray irradiation experiment and high temperature stability measurements.[69] In fact, knock-on structural change in Si can be readily induced by an electron beam at the imaging energy (200 KeV),[94] and the amorphization process can be induced.[86,95] This accounts for the switching degradation after beam exposure (Fig. 67b) as structural changes along the entire filament are induced. While this is a further indication of structural change-induced conductance switching in the Si filament, it also implies that the structural transition needed for the switching can be subtle.

4.3 Summary

From static imaging by CNT-assisted localization to *in situ* imaging using C-SiO_x thin-wall structures, the Si-rich filament in SiO_x resistive switching device is visualized. In particular, the study in *in situ* imaging provides an overall picture of the

intrinsic resistive switching in SiO_x. The electroforming is through the $SiO_x \rightarrow Si$ process with the semi-metallic Si state identified. The switching is indicated to be through the transition between the semi-metallic and amorphous Si forms. It also provides a general overview of electrical breakdown in silicon oxides. The degradation of the resistive switching state to a nonswitchable metallic state (hard breakdown[96]) in SiO_x is likely to be associated with the further aggregation of the metallic Si forms. The method described here can also be applied to other resistive switching materials for mechanistic investigation.

Chapter 5

Silicon Oxide is a Non-Innocent Substrate in Molecular Electronics and Nanoelectronics Studies

5.1 Introduction

As covered in Chapters **1** and **2**, the study of the resistive switching phenomena in SiO_x initially started from a mechanistic investigation of carbon-material-based memory on SiO_x substrates. With the intrinsic conduction and switching in SiO_x discussed and largely revealed (Chapters **2-4**), here we turn back to discussing the implications of SiO_x switching in other nanoelectronic devices.[97]

Because of its good insulating properties and mature technologies in fabrication, SiO_x has long been used as a passive and insulating material in electronics. In the construction of typical two-terminal electronic devices, it is frequently used as a supporting substrate for a pair of planar electrodes, or as an insulating spacer between a pair of vertical ones. Topologically, this E-SiO_x-E (E denotes electrode) system defines a gap structure across which material of interest can be bridged and electrically measured. Since SiO_x ordinarily contributes negligibly to conduction, the measured electrical properties are solely attributed to the material of interest. Through this approach, electrical transport properties in various molecules and nanomaterials have been investigated.[47-49,55,65,77,78,98-103]

However, it has been shown in the previous chapters that this traditionally passive SiO_x can be readily converted into an electrically active material for resistive-switching memory.[25,52,69,74] The conduction and resistance change occurs through voltage-driven formation and modification of a pathway of silicon (Si)

nanocrystals (NCs) embedded in the SiO_x matrix, with SiO_x itself also serving as the source for the formation of Si NCs.[69] This mechanistic picture reveals the intrinsic property of conduction in SiO_x and therefore results in electrode-independent resistive switching in SiO_x.[52] While efforts have been directed toward SiO_x-based memory device fabrication, performance and mechanism investigation,[25,69] little attention has yet been paid to the implications of this conduction upon other electronic systems that use SiO_x as a device component. In particular, in molecular systems, the spacing between the electrodes tends to be close in order for the molecules, either monolayers or multilayers, to be bridged between the pair of electrodes. Consequently, at modest voltages, high local electrical fields are attained in the gap defined by the pair of electrodes. It is then of critical importance to determine whether the measured electrical phenomena are truly the result of molecular conduction or resulting from SiO_x conduction induced by the high electrical field.

In this chapter, we firstly demonstrate resistive switching to a thin layer of SiO_x (thickness $t \geqslant 7$ nm). Depending on the history and sweep mode, we show in details how one can obtain various nonlinear current-voltage (*IV*) behaviors, which essentially point to the same phenomenon and underlying mechanism. The nonlinear features in the *IV* curves include conductance peaks and current hysteresis. At the post soft-breakdown state, we further show that negative differential resistance (NDR) and current hysteresis can be obtained at a lower voltage range (below the resistive-switching voltage range). The electrical phenomena are explained by the

filamentary conduction nature in SiO_x. Finally, we show different current hysteretic behaviors from a native silicon oxide surface (t ~ 1.5-3 nm). All these electrical behaviors can largely mimic electrical phenomena observed in molecular and nanoelectronic systems, suggesting substantial caution must be paid when studying conduction in nanoscale systems that use SiO_x as an isolating layer. Starting with a plausible molecular conduction, we then show that this nonlinear conduction is actually from the SiO_x itself and underlies the resistive switching in SiO_x. This is done by reproducing the same effect in a bare system without the molecules. Furthermore, by employing a carbon-nanotube network to mimic a nanoelectronics study, we show that the initial conduction assists and eventually evolves into SiO_x conduction. The electrical behavior and properties of SiO_x conduction are further discussed, providing potential guides to allow SiO_x conduction to be distinguished from other nanoelectronic behaviors. It should be noted that previous studies[25,52] have mainly focused on the memory properties of SiO_x with layer thicknesses > 30 nm, whereas the electrical phenomena discussed here cover the SiO_x thicknesses below 20 nm and down to 2 nm (surface native oxide), closer to molecular dimensions.

5.2 Main Discussion

5.2-1 Molecular Effect?

To sandwich molecules between a pair of electrodes, vertical polySi-SiO_x-polySi ($x \sim 2$) stacking structures with diameters of 100 μm were fabricated as illustrated in Fig. 71a. Highly doped polySi layers ($\rho < 0.005$ Ω·cm, thickness = 70 nm) are used

here as both top and bottom electrodes to exclude any effects due to motion of metal from the electrodes.[104,105] The two electrodes were spaced by a SiO_x layer with a thickness of 10 nm. By etching away some portion of the SiO_x at the vertical edge in a 10:1 buffered oxide etch (J. T. Baker), a vertical nanogap system was defined and molecules can be assembled in the nanogap.[102] This structure is similar to other vertical molecular systems in which SiO_x layers were used as insulating and supportive spacers between the top and bottom electrodes.[97-99] 3-Aminopropyltriethoxysilane (APTES) molecular layers at an estimated thickness of 10 nm were then assembled onto the vertical SiO_x surface in the nanogap, following a process described in the literature.[106] All of the electrical characterizations were performed under vacuum (10^{-5} Torr) at room temperature. The successful assembling of the molecules is indicated by the increased conduction compared to that of a pair of bare electrodes (inset in Fig. 71b). During a subsequent series of consecutive voltage sweeps from -12 V to +12 V, the current level gradually increased until it reached a certain value after several voltage sweeps; during this process, nonlinear *IV* curves featuring conductance peaks at ~ ±7.5 V were persistently observed (Fig. 71b). The nonlinear behavior was approximately symmetric in the negative and positive voltage regions, and was very similar to that observed in OPE molecules assembled in metal nanogaps on a SiO_x substrate.[100]

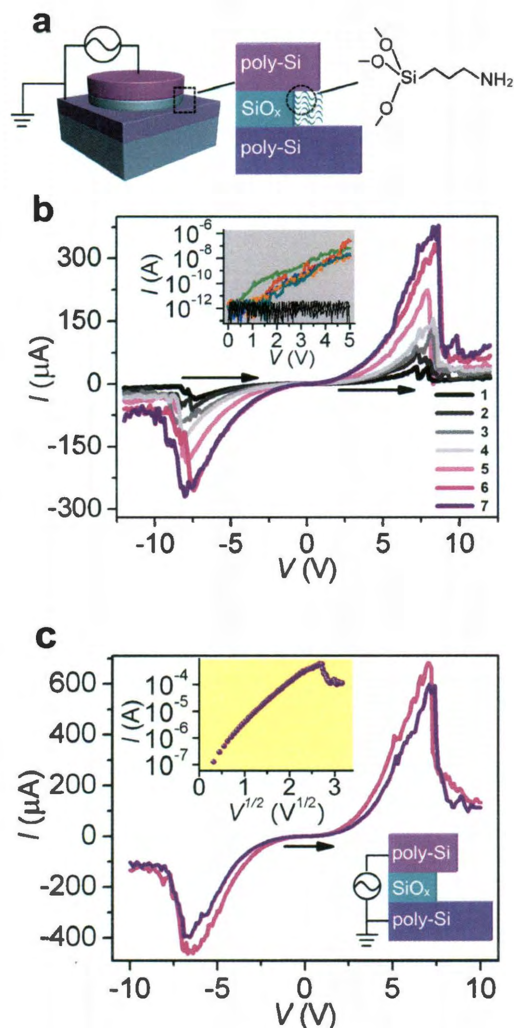


Figure 71. (a) Left panel: Schematic of a vertical polySi-SiO_x-polySi structure (70 nm-10 nm-70 nm) and the electrical-characterization setup. The diameter of the structure is 100 μm. Right panel: an enlarged schematic of the nanogap defined at the vertical edge in which APTES molecular layers are assembled. (b) Consecutive voltage sweeps (-12 V → 12 V) in a device with APTES molecular layers as shown in (a) The numbers indicate the voltage-sweep orders. Inset shows the conduction before (black curves) and after (color curves) APTES assembling in several devices, with each curve corresponding to one device. (c) *IV* curves (-10 V → +10 V) in a bare polySi-SiO_x-polySi device without molecules. Note that the device was thermally annealed at 600 °C for 10 mins in a reducing environment (Ar/H_2 =450/150 sccm) prior to the electrical characterization. The top inset shows one of the *IV* curves in the

positive bias region in a $log(I)$-$V^{1/2}$ format. The bottom inset shows a schematic of the vertical edge on which no molecules are assembled.

A control experiment in which no APTES molecules were assembled in the polySi-SiO_x-polySi nanogap shows almost the same *IV* curves (Fig. 71c). The absence of molecules here indicates that the electrical behavior in the previous system was not intrinsic to the molecules. Instead, it resulted from the soft breakdown of the SiO_x layer at the vertical edge[69] region by the high electrical field built in the nanogap, as has been discussed in previous chapters. The gradually increased current level upon continuous voltage sweeps (Fig. 71b), deviating from the initial conduction (inset in Fig. 71b), was a signature of the electroforming process in SiO_x. Similar electrical behaviors were first described in the 1960s in silicon-rich M/SiO_1/M (M denotes metal) sandwiched systems.[107] While different models were proposed for the mechanism,[20] the exclusive use of metal electrodes often led to a mechanistic picture of conduction by metal defects injected from the electrodes.[107] The defective silicon-rich SiO_1 system and the extrinsic metal-filamentary picture have likely contributed to the neglect of the potential conduction from SiO_x in other electronic systems, where x is usually close to 2 to ensure a good insulating property. As discussed in the previous chapter,[69] we showed the details of SiO_x-generated conduction: the voltage-driven electrochemical processes can induce local reduction of SiO_x to form Si nanocrystalline pathways and lead to increased conduction and resistive switching intrinsic to SiO_x. The formation of this localized conduction

usually occurs at the SiO_x surface region, which is more defective and easier to induce soft breakdown. Here it was revealed[25,69] to be at the etched vertical edge of the SiO_x layer. The soft breakdown can be readily induced in SiO_x with various x values (*e.g.*, $1 < x \leqslant 2$) and the formed electrical behaviors are largely electrode-independent.[52]

5.2-2 SiO_x Related Non-Linear Behaviors

In light of the Si-filament conduction, the nonlinearity in the *IV* curves can be a result of voltage-driven structural changes in the conducting pathways or filaments. For example, the conductance increase and decrease correspond to the construction and destruction of the conducting filaments, respectively. Therefore, the resistance of the SiO_x depends on the history of the voltage sweeps that modified the filaments. For example, if a voltage sweeps above V_{max} (the voltage at the conductance peak) and then drops fast to 0 V, the resultant resistance of the SiO_x corresponds to the value at this voltage and can be estimated through an "extrapolation rule".[20] This is illustrated in Fig. 72a in which the *IV* relationship is presented in a $log(I)$-$V^{1/2}$ format, since generally the conduction in SiO_x is dominated by tunneling having the characteristic of $log(I) \propto V^{1/2}$ (see upper inset in Fig. 71c).[20,107] If a voltage sweeps to V_1 and then drops quickly to 0 V, it is expected that the conductance of the SiO_x has been changed to G_1 which can be estimated by drawing an extrapolation line parallel to the initial *IV* curve in the $V < V_{max}$ region (Fig. 72a). In a similar way, lower conductance G_2 can be achieved by sweeping to a voltage V_2 ($V_2 > V_1$). This rule is well-demonstrated in the actual *IV* curves in Fig. 72b in which each starting conductance (dashed curves)

depends on the previous voltage sweep (solid curves) through the "extrapolation rule". The *IV* curves in Fig. 72b also define the 'read', 'set', and 'reset' regions that are usually identified in resistive-switching devices. The 'reset" region is at $V > V_{max}$ as voltages in this region reset the SiO_x to lower-conductance states. And the 'set' region begins at a threshold voltage V_{th}, at which the lower conductance suddenly increases and deviates from the original $log(I) \propto V^{1/2}$ curve in the 'read' region. For the above reasons, multilevel nonvolatile resistive memory can be realized by applying voltage pulses of different magnitudes (see Fig. 72c).

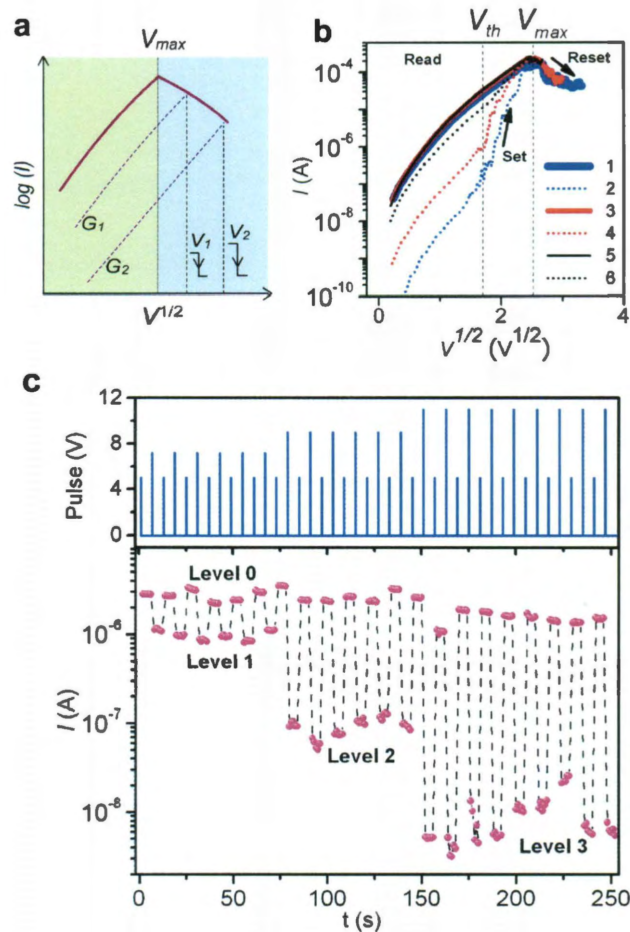


Figure 72. (a) An illustration of the "extrapolation rule" in a $log(I)$-$V^{1/2}$ format. (b) Consecutive *IV* curves in a bare vertical polySi-SiO_x-polySi device as illustrated in Fig. 71c (lower inset). The numbers indicate the voltage-sweep orders. The solid curves are voltage sweeps from 0 to a value above V_{max}, with blue, red, and black curves correspond to 0 V → +11 V, 0 V → +9 V, and 0 V → +7 V, respectively. The dashed curves are voltage sweeps from 0 V to a value (+6 V) close to V_{max}. 'Read', 'Set', and 'Reset' regions are defined by V_{th} and V_{max} as shown in the figure. (c) Top panel: A series of voltage-pulse sets of (+5 V, +7 V), (+5 V, +9 V), and (+5 V, +11 V) working as programming voltages. Bottom panel: corresponding memory states read by a +1 V pulses. Note the programming current is not shown here. The data indicates that a set voltage of +5 V programs the device into the ON state (level 0), whereas reset voltages of different magnitudes (+7 V, +9 V, +11 V) program it into different OFF states (Level 1, Level 2 and Level 3).

For the above discussion, depending on the voltage-sweep history and mode, different *IV* behaviors can be observed in SiO_x. For example, for a backward voltage sweep starting from the 'reset' region to 0 V, the *IV* curve is always in an ON state in the 'read' region as it eventually bypasses the 'set' region (Fig. 73a). However, for forward voltage sweeps starting from 0 V to a reset voltage, after the first sweep, the subsequent sweeps always have OFF states in the 'read' region since each previous sweep ends at the 'reset' region (Fig. 73b). Similarly, in double-sweep modes, if initially the device is in an ON state, no current hysteresis is produced (Fig. 73c). If initially the device is in an OFF state, hysteresis is produced (Fig. 73d). This last type of sweep has been frequently used[25,52,69,108,109] as characteristic resistive-switching *IV*

curves since it indicates both the programming regions and ON/OFF ratio. Similarly, the electroforming process that converts the pristine SiO_x into a resistive-switching state can also have different *IV* evolutions with respect to different voltage-sweep modes (see Fig. 74).

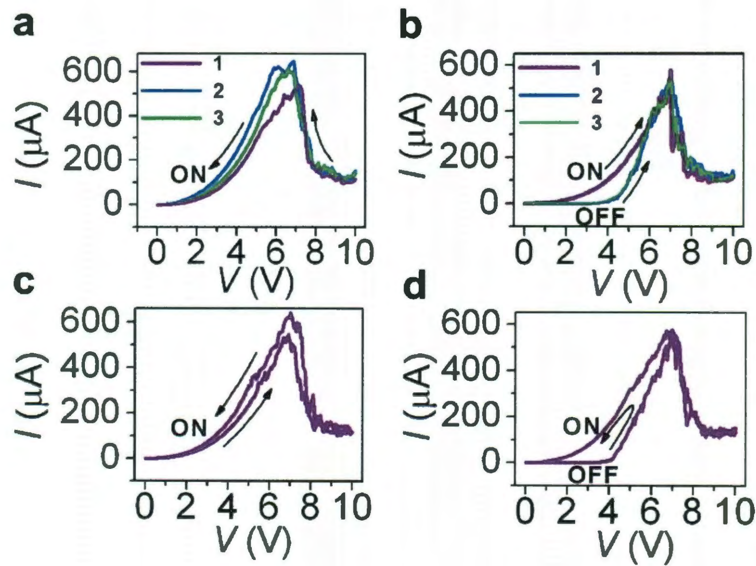


Figure 73. *IV* curves in a vertical polySi-SiO_x-polySi (70 nm-10 nm-70 nm) device by different voltage-sweep modes: (a) single backward sweeps (+10 V → 0 V); (b) single forward sweeps (0 V → +10 V); (c) Double sweep (0 V → +10 V → 0 V) starting with an ON state; (d) double sweep (0 V → +10 V → 0 V) starting with an OFF state. The arrows indicate the sweep directions and the numbers indicate the sweep orders.

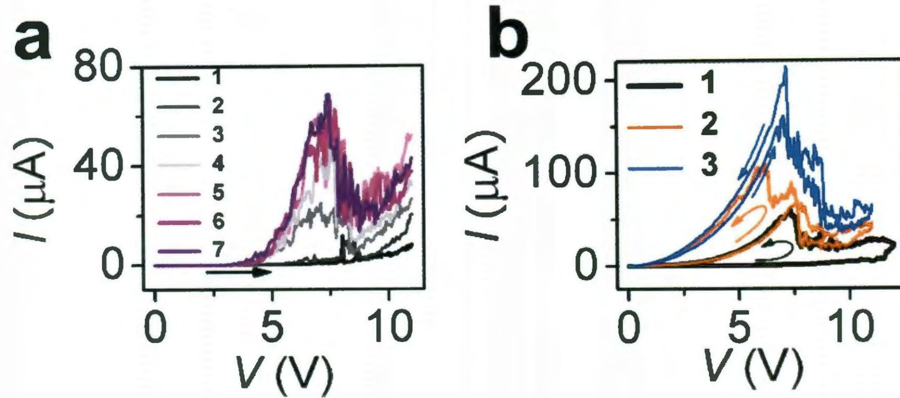


Figure 74. Electroforming processes in vertical polySi-SiO_x-polySi (70 nm-10 nm-70 nm) devices by different sweep modes. The devices have the same structure and parameters as illustrated in the main article in Fig. 71c. (a) An electroforming process by consecutive forward voltage sweeps (0 V → +11 V). Since each voltage sweep ends in the reset region, the formed device is always in an OFF state. (b) An electroforming process by consecutive loop voltage sweeps (0 V → +12 V → 0 V). Since each voltage sweep finally bypasses the set region, the formed device is always in an ON state. The arrows indicate the voltage-sweep directions and the numbers indicate the voltage-sweep orders. An electroforming process by consecutive backward voltage sweeps (*e.g.*, + 12 V→ 0 V) is similar to that described in Fig. 71b in the main article.

The above resistive-switching *IV* curves in SiO_x feature conductance peaks that resemble those in NDR effects. However, it should not be classified as the specific NDR that results from resonant tunneling.[110] As the underlying cause for resistive switching or conductance change in SiO_x is voltage-driven modification of the conducting filament, the *IV* curves are sweep-history and sweep-direction dependent (as shown in Fig. 73), whereas resonant-tunneling based NDR should be not.

Nevertheless, in the later context we will show that SiO_x can still produce similar resonant-tunneling NDR at a lower voltage region.

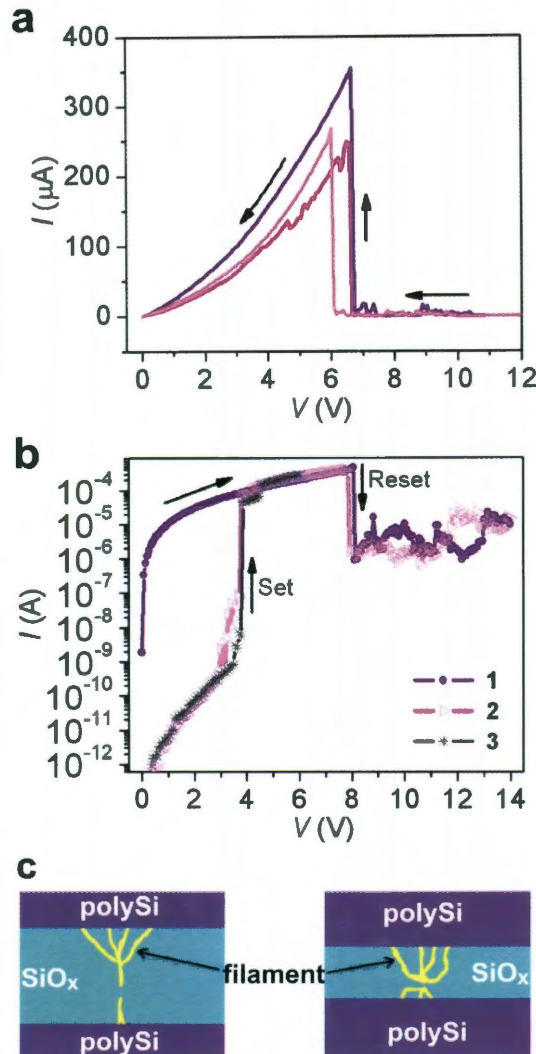


Figure 75. (a) Backward voltage sweeps (+12 V → 0 V) in a vertical polySi-SiO_x-polySi (70 nm-40 nm-70 nm) device, showing steep conductance peaks. (b) Forward *IV* curves from the same device in (a), showing sharp set and reset threshold voltages. The numbers indicate the sweep order. (c) Illustrations depicting the SiO_x-layer thickness effects on the development of conducting filaments and thus the OFF current. Left panel: An OFF state from a fully-developed filament in a comparatively thick SiO_x layer. Right panel: An OFF state from a less effectively

developed filament in a thin SiO_x layer. The development of the single filamentary strand in the thick SiO_x layer ensures a low OFF tunneling current, while the lack of this single filamentary strand in the thin SiO_x layer results in an increased cross-section area of tunneling, thus an increased OFF current.

The conductance peak in SiO_x conduction can be very sharp (Fig. 75a), as have been shown in previous chapters, too. Consequently, the characteristic resistive-switching *IV* curves feature sharp set and reset threshold voltages (Fig. 75b). As resistive switching in SiO_x is through filamentary conduction, the differences in the *IV* curves can be considered as the consequence of different evolutions in the filament. In the proposed mechanistic picture of an electrochemical redox process of $Si \leftrightarrow SiO_x$ at the resistive-switching site,[69] it can be understood that the effectiveness of this process, even in a single filament, can commensurately modulate the conductance change. For example, a more effective oxidation process of $Si \rightarrow SiO_x$ at the resistive-switching site is expected to cause more abrupt decrease in the OFF conduction. The dynamics of the resistive-switching process, including the degree to which redox switching of Si/SiO_x can be cooperative at multiple sites, may well be affected by internal stress distributions associated with the glassy SiO_x structure.[111] A restricted film thickness is likely to hinder the formation of a single filamentary strand (as illustrated in Fig. 75c), resulting in an increased cross-sectional area of tunneling in the OFF state, thus the increased OFF current. This is consistent with our observation that the average ON/OFF ratios in thin SiO_x film (10 nm) was typically within 10^3, compared to ratios exceeding 10^4 in thicker SiO_x film (40 nm), mainly

because of the increased current in the OFF states. It also raises the question: At what thickness does SiO_x still demonstrate resistive switching and related nonlinear behavior? Our experiments indicate that similar reproducible electrical phenomena can be induced in SiO_x with thicknesses ranging from 7 nm to 200 nm (Fig. 58a), covering a majority of nanogaps defined on SiO_x for molecular and nanoelectronic systems that have been studied.

5.2-3 Material-Assisted Forming

With the assistance from other conducting pathways, this SiO_x thickness could extend far beyond 200 nm. We used a network of multiwalled carbon nanotubes (MWCNTs) to mimic a random molecular layer or other conducting nanomaterials on a Si substrate capped with 200 nm thermal-grown SiO_x ($x \sim 2$, Silicon Quest International, Inc.), and patterned the network with two electrodes over 5 μm apart (Fig. 76a). By sweeping to +14 V, multiple sudden conductance decreases are observed (Fig. 76b) as a result of electrical breakdowns in the MWCNTs. This is also visible in the physical breaking of MWCNTs (Fig. 76c, indicated by green arrows). Upon further voltage sweeps, the SiO_x between certain nanogap defined by two broken ends of MWCNT can form soft breakdown and be electroformed to a resistive-switching state. This process is always accompanied by visible morphological change to the SiO_x at the nanogap region (left panel in Fig. 76c), which is a signature of the electroforming process in various resistive-switching materials.[20,69] Hence, starting with a conduction initially coming from the

MWCNT-network, the conduction eventually evolves into reproducible nonlinear behavior and resistive switching coming from SiO_x (Fig. 76d,e), with the broken MWCNT network merely serving as effective nano-spaced electrodes.

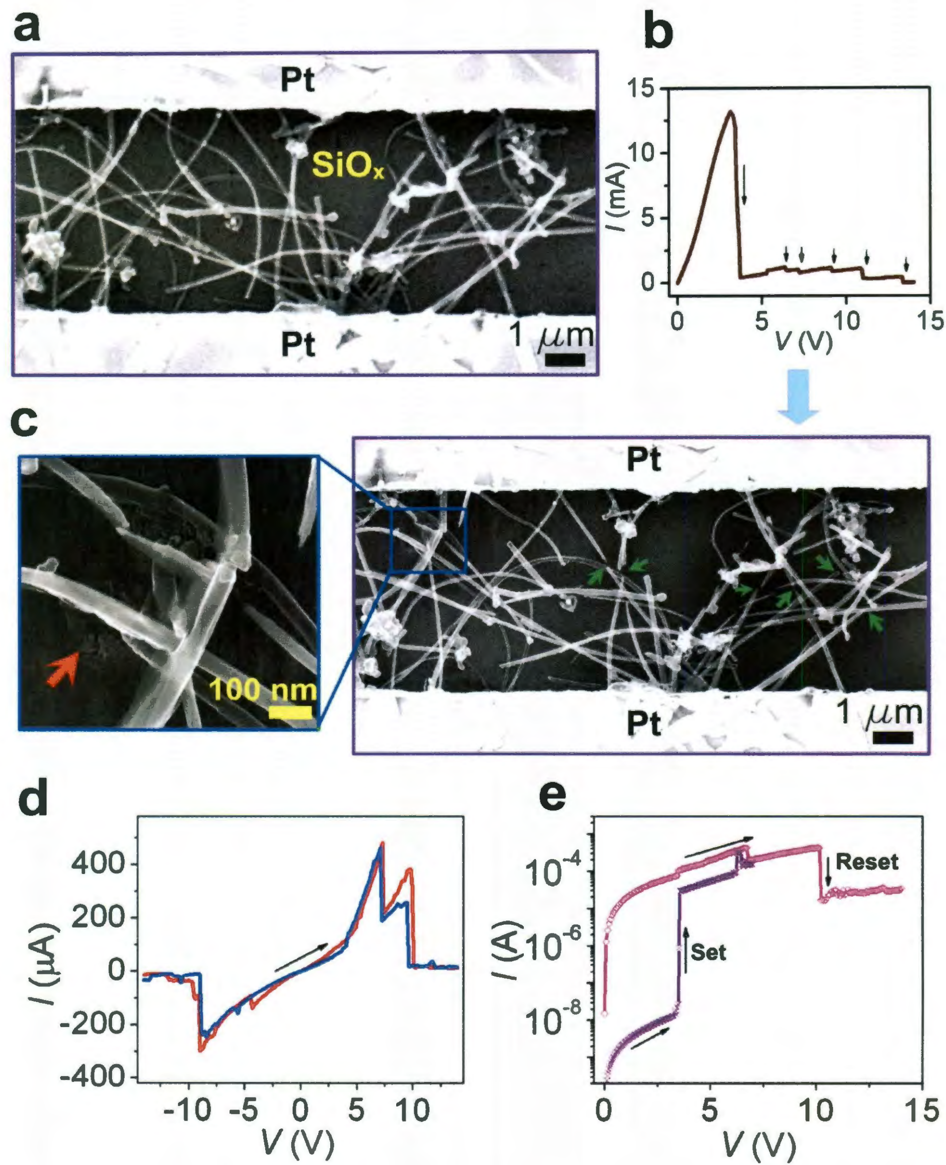


Figure 76. Resistive switching and related nonlinear conduction in a MWCNT network on a Si substrate capped with 200 nm thermal-grown SiO_2. (a) A scanning electron microscopy (SEM) image of the random MWCNT network. (b) Initial voltage sw sweep (0 V → +14 V). The black arrows indicate sudden current drops, or electrical breakdowns in MWCNTs. (c) SEM image of the same MWCNT-network

device after the voltage sweep in (b) The green arrows indicate broken regions in different MWCNTs. The inset on the left panel is a zoomed-in picture of the MWCNT network. It shows the broken regions of MWCNTs, along with observable damage to the underlying SiO_2 substrate (indicated by the red arrow). (d) *IV* curves featuring conductance peaks in the same electroformed device. The multiple peaks are likely caused by multiple MWCNT-SiO_x-MWCNT resistive-switching sites. (e) Characteristic resistive-switching *IV* curves in the same device.

The above MWCNT network offers a vivid example of how conductive molecular layers or nanomaterials can assist the formation of SiO_x conduction; the disruption of molecular layers or nanomaterials, either by local electrical breakdown or nonuniformity during assembly, helps to build up a high local electrical field that leads to a soft breakdown in the SiO_x layer. As the resultant conduction and resistive switching are intrinsic properties of SiO_x, they can be induced in the SiO_x by different molecules or other exogenous materials atop the SiO_x substrate.[52] This SiO_x soft breakdown-induced conduction and resistive switching might be the cause of various qualitatively similar electrical behaviors in molecule layers,[100,101] carbon materials,[47,49,65,112] nanowires,[48,103] and bare nanogaps,[55,77,78] in which little attention, if any, was formerly paid to the SiO_x substrates.

Besides building up high local fields, the initial conduction from molecules or nanomaterials also provides current local heating which could assist the electroforming in SiO_x since thermal annealing was found to introduce more defects

at the SiO_x surface.[25,69] These introduced defects could serve as electron hopping centers so that electroforming is more easily induced at a voltage below the hard-breakdown threshold. This is also the case for the bare polySi-SiO_x-polySi structures (Fig. 71c) in which thermal annealing (600 °C, 10 min, Ar/H_2 = 150/50 sccm) prior to electrical characterizations was adopted to facilitate the electroforming process. With a layer of APTES molecules, which introduce both enhanced local electrical field and current local heating, the system can be readily electroformed as described in Fig. 71a without thermal annealing. Not surprisingly, coating the bare polySi-SiO_x-polySi structure with a thin layer (5 nm) of amorphous carbon can serve the same role and leads to the electroforming of SiO_x and similar nonlinear electrical behavior (Fig. 77).[49]

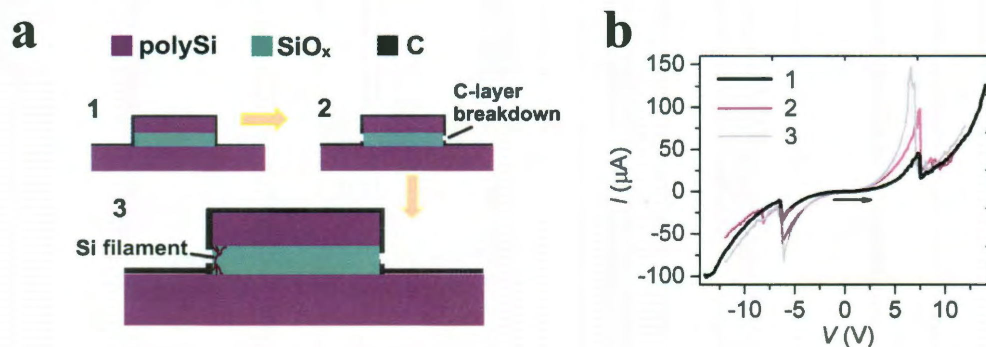


Figure 77. Resistive-switching *IV* curves in a vertical polySi-SiO_x-polySi (70 nm-10 nm-70 nm) device coated with 5 nm-thick amorphous carbon. (a) Schematics showing the C layer assists the electroforming in the SiO_x layer. 1. The initial C-coated structure. 2. Electrical breakdown in the C layer creates disruptions at the vertical SiO_x edge. 3. The disruption in the C layer enhances the local filed and induces soft breakdown at the vertical SiO_x edge. An electroforming process is then initialized with the formation of Si-NC filament. (b) The actual electroforming process in an

actual C-coated device. The arrow indicates the voltage-sweep direction and the numbers indicate the voltage-sweep orders. This is analogous to switching behavior observed in related systems.[49]

Note that while electrical breakdown in bulk SiO_x usually requires an electrical field larger than 10 MV/cm, a SiO_x surface in contact with other exogenous nanomaterials, or that is subjected to thermal annealing, has more defects and is therefore an easier material in which to induce soft breakdown at a lower electrical field. Consequently, the conduction in the vertical polySi-SiO_x-polySi is found to be localized at the vertical SiO_x edge.[69]

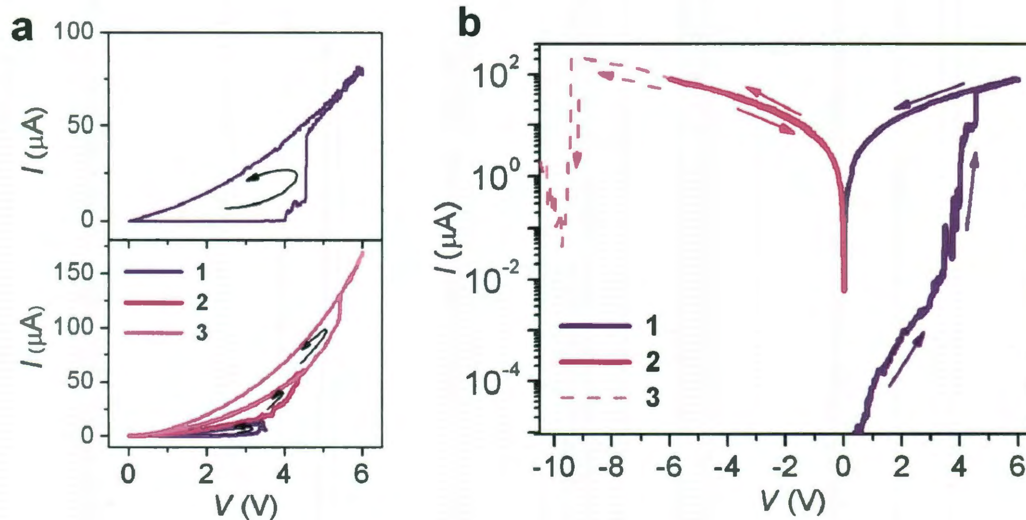


Figure 78. (a) Top panel: a hysteretic *IV* curve featuring a set operation in a vertical polySi-SiO_x-polySi device with 40 nm SiO_x. Bottom panel: multiple hysteretic *IV* curves featuring a series of multi-stage set operations in a vertical polySi-SiO_x-polySi device with 10 nm SiO_x. The arrows indicate the sweep directions and the numbers indicate the sweep orders. (b) *IV* sweeps in both polarities in a polySi-SiO_x-polySi

device with 40 nm SiO_x. Curve 1 shows a set process (0 V → +6 V → 0 V) in the positive bias region. Curve 2 shows a subsequent voltage sweep (0 V → -6 V → 0 V) in the negative bias region, with no reset operation incurred. Curve 3 shows the next voltage sweep (0 V → -12 V) that triggers a reset operation at ~ -9 V.

While the appearance of a conductance peak requires a voltage sweep above V_{max}, current hysteresis can be readily produced in the 'set' region with $V > V_{th}$ (see V_{th} definition in Fig. 72b). For example, starting from an OFF state, any voltage sweep to a value above V_{th} incurs the set process and thus current hysteresis. The conductance increase in the hysteretic loop can be abrupt (top panel in Fig. 78a) or gradual featuring multi-stage set processes (bottom panel in Fig. 78a). These behaviors cannot only mimic current hysteresis in molecular systems,[113] but also in mechanical switches where similar vertical M-SiO_x-M stacking structures were adopted.[114,115] As V_{set} is smaller than V_{reset}, this type of hysteresis is always unidirectional (counter-clockwise) toward a higher-conductance state. The non-volatility also determines that the same hysteresis is not reproducible before a reset operation is performed. In particular, a reset operation cannot be performed by sweeping to the opposite polarity of - $|V_{set}|$ (Fig. 78b), but needs to sweep further to - $|V_{reset}|$. This features the typical unipolar resistive switching that is only voltage-magnitude dependent but not polarity dependent. It should be noted that some resistive-switching systems[116,117] were presented similarly in both polarities, but these are essentially unipolar behaviors as described in Fig. 78b.

The underlying cause for all the above electrical phenomena is voltage-driven formation and modification of conduction filaments (Si filament) embedded in the SiO_x matrix. A certain minimum voltage is required in order to electrochemically modify the conducting pathway. Generally, the conductance peak appears at $|V_{max}| > 3$ V, which indicates that resistive-switching behavior below 3 V is unlikely from SiO_x. However, there is no clear maximum V_{max}, since interface resistance can reduce the actual voltage drop across the SiO_x, thus pushing V_{max} above 10 V.[52] The *IV* curve in the 'read' region ($V < V_{th}$) is comparatively smooth and dominated by tunneling. Above V_{th}, as voltage-driven modifications of the conducting filaments begin, current fluctuations begin. These fluctuations alone produce various local conductance peaks (*e.g.*, see Fig. 78) which are not reproducible. They also persist in the electroforming process prior to the formation of resistive-switching state (Fig. 74). Therefore, careful attention should be paid in molecular and nanosystem characterizations, in which the reproducibility of the *IV* curves are sometimes not described or are neglected. The resistive switching in SiO_x needs to be in an oxygen-deficient environment, and cannot be performed in ambient environment. This may be due to the Si-filamentary nature where current local heating induced oxidation prevents the conductance modulation. However, once "programmed" by electroforming, the resistance states are air-stable with a retention time projected to be above years. This can be a good point of difference from some charge-based molecular memory systems in which the states decay faster.[102,116,118]

5.2-4 NDR and Current Hysteresis at Low Voltage

Although the mechanisms for the resistive switching and related nonlinear conduction in various molecular and nanomaterial systems are largely unknown and debatable,[119] many have turned out to be through localized filamentary conduction.[119-121] In this form, the resistance change can be generally viewed as a result of electronic structural change by doping or electrochemical reactions[119] in the conducting pathways. Therefore, the conductance can be modulated in a nonvolatile manner. Meanwhile, the energy gaps between the highest molecular orbitals (HOMO) and lowest unoccupied molecular orbitals (LUMO) can produce NDR behavior through resonant tunneling,[122-124] an effect similar to that in a resonant tunneling diode. Since resonant tunneling results from energy-level alignment between the electrodes and the molecular orbitals modulated by an external bias, the conductance change is volatile. Also, as tunneling current decays exponentially with molecular dimensions, resonant tunneling is usually observed in monolayer or few-layer molecules at low voltage bias (< 3 V) with limited currents.[125,126] These aspects differ from the resistive-switching related nonlinear behaviors in the SiO_x discussed above.

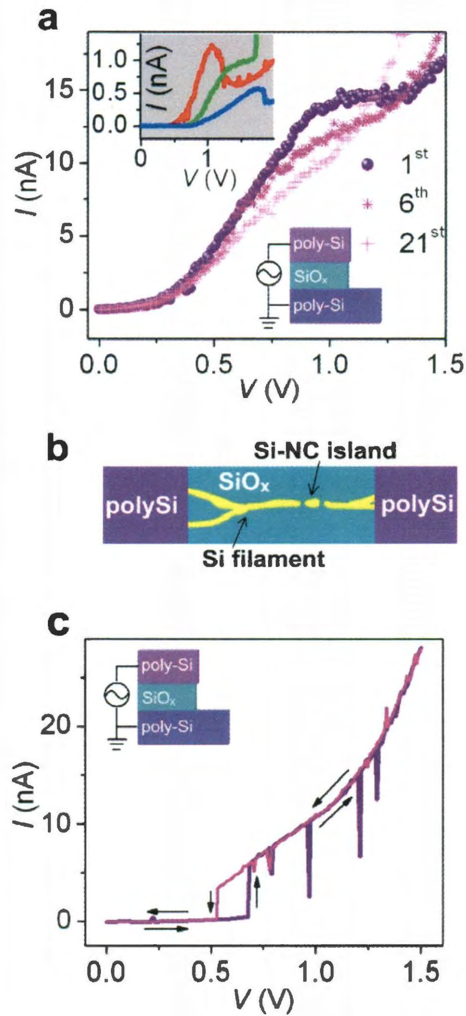


Figure 79. (a) NDR at low voltage in a polySi-SiO_x-polySi device (illustrated in the bottom inset) having the same structure and parameters as described in Fig. 71c. The numbers indicate the numbers of voltage sweeps, showing a gradual disappearance of the NDR on the 21st sweep. Top inset shows three different NDR curves obtained in a same device at different OFF states programmed by reset processes. (b) A schematic showing an isolated Si-NC island in the filamentary path. (c) Current hysteresis at low voltage (0 V → 1.5 V → 0 V) in a polySi-SiO_x-polySi device (illustrated in the top inset) having the same structure and parameters as described in Fig. 71c. The arrows indicate the voltage-sweep directions.

Nevertheless, we find that at a post soft-breakdown state, SiO_x can also show similar resonant tunneling at a low voltage region (Fig. 79a), with the conductance-peak location and current level close to those observed in molecular systems.[125,126] The appearance of this behavior can be understood based on a mechanistic picture of conduction through an aligned Si-NC pathway.[69] During the process of electroforming, or at an OFF state, the discontinuity of the Si-NCs gives rise to the possibility of forming an isolated Si-NC island along the pathway (Fig. 79b). The confinement in the Si-NC island results in discrete energy levels, thus the resonant tunneling effect. This proposed mechanistic picture is indeed supported by the experimental observation of NDR in a Si quantum dot array.[127] Since a read voltage (*e.g.*, < 3 V) is not expected to induce structural change in the filament, the *IV* curve is reproducible (Fig. 79a). The gradual degradation of the NDR upon continuous voltage sweeps (Fig. 79a), which was also observed in molecules,[128] may be due to charge-trap effects. As the morphology of the filament can be altered during electroforming or after different programming processes, variations in this resonant-like NDR are expected, even in the same device at different stages of the filament evolution. This is shown in the inset in Fig. 79a; three different NDR curves from the same SiO_x device can be obtained after different reset processes. The appearance of this resonant-like NDR behavior in SiO_x is comparatively low (within 5% in different OFF states), while the rest are through typical tunneling as described before (Fig. 72b). It should be noted that, due to the semi-analog conductance

modulation through multi-stage set (Fig. 78a) or reset processes (Fig. 72c) described above, various resistance states ranging from kΩ to GΩ can be achieved in SiO_x. These conductions, though perhaps without NDR, can still mimic non-ohmic conduction in molecules.[98,99]

SiO_x can also produce other effects in the low voltage region. Fig. 79c shows an *IV* curve with an abrupt conductance jump at ~0.65 V and, when tracking back, a sudden conductance drop at ~0.5 V, producing a hysteresis window of ~0.15 V. Similar electrical behavior has also been observed in single molecules.[129] The actual cause for this behavior in SiO_x needs further investigation. It is likely that some sudden trapping and de-trapping events happen upon certain threshold voltages, thus rapidly modulating the conductance.

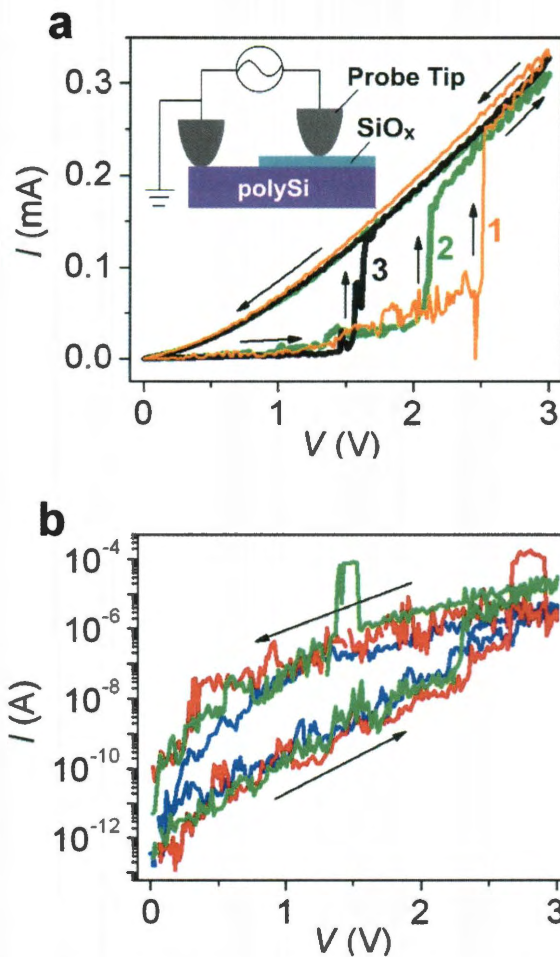


Figure 80. Electrical phenomena from surface native oxide. (a) Hysteretic *IV* curves from a surface native-oxide layer (1.5-3 nm thick). The numbers indicate the voltage-sweep order, and the arrows indicate the voltage-sweep direction. The inset is a schematic of the electrical setup. (b) Another series of hysteretic *IV* curves from a surface native-oxide layer, with the arrows indicting the voltage-sweep direction.

Finally, we tested a native-oxide layer (1.5-3 nm) atop a conducting polySi surface. Unlike previous systems where the SiO_x layers are intentionally grown, here the SiO_x layer is naturally formed on the Si surface in an ambient environment. This is

relevant to some Si-electrode based molecular systems[130,131] in which, though SiO_x may be not intentionally used, a native-oxide layer will inevitably be produced when the electrodes are fabricated.[124,128,132] We tested the electrical property of this native-oxide layer by directly landing two probe tips (tip diameters are ~ 20 um) on the polySi surface (see illustration in inset in Fig. 80a). We first formed a good ohmic contact between one tip and the polySi surface by a voltage sweep to a high value (*e.g.* > 5 V) to induce a hard electrical breakdown in the native-oxide layer. We then landed the other tip to a new location. Hence the electrical phenomena come from one tip-SiO_x-polySi interface. Fig. 80a shows a series of hysteretic *IV* loops from one of the interfaces we tested. Here the hysteresis differs from a set process in the resistive-switching curves (Fig. 78a) in that after each sweep loop, the subsequent sweep still starts with an OFF state, featuring the reproducibility and volatile property. The observed phenomena are very similar to those hysteretic behaviors observed in molecular systems at low voltage.[133,134] In addition to clear conductance-increase steps in Fig. 80a, Fig. 80b shows another series of current hysteretic *IV* curves with large current fluctuations from a native-oxide interface. Note that in both electrical phenomena, the native-oxide layer has not yet experienced a hard electrical breakdown, which is indicated from the reproducibility of the hysteresis and low conductance. Hence, the phenomena are likely to be charge-trap related. Hard electrical breakdown in the native-oxide layer is induced at a voltage above 3 V, after which the interface is permanently in an ohmic-contact state with no hysteretic behavior. For this reason, resistive switching and related nonlinear behavior as

described before (Fig. 72) are not observed in native-oxide layers.

5. 3 Summary

In this chapter, we have demonstrated various electrical phenomena including resistive switching and related nonlinear electrical behaviors, current hysteresis and NDR intrinsic to a thin layer of SiO_x. These behaviors can largely mimic various electrical phenomena observed in molecules and other nanomaterials. The underlying cause for these effects is voltage-driven and high-electrical-field induced soft breakdown in the SiO_x layer. In particular, this soft breakdown can be readily induced by unintended factors, such as defects in a SiO_x surface, material-assisted local electrical-field enhancement and current local heating as described in this article. Many other studies have been conducted in detailing the physical mechanism of SiO_x breakdown and conduction.[135-138] The study and results call for care when studying conduction in electronic systems with SiO_x as a nominally passive component. The forming processes, behaviors, and mechanisms have been discussed in detail, providing a potential guide to distinguish electrical phenomena in molecules and nanomaterials of interest from those in SiO_x.

Chapter 6

Memory Effect in Single-Walled Carbon Nanotubes: Charge Trap at the SiO_x/Carbon-Nanotube Interface

6.1 Introduction

The resistive switching and memory effects discussed in previous chapters are the intrinsic properties of SiO_x. In other words, SiO_x alone serves the active role as the functional element. Here we divert from its active role and discuss its passive role as a charge-trap medium to construct charge-based two-terminal nonvolatile memory.[118]

Various nanowires,[43,45] due to their quasi one-dimensional structures, have been studied to show new/enhanced functions and serve as proofs of concept for device miniaturization from bottom up. In particular, single-walled carbon nanotubes (SWNTs) have received great interest for their extremely small diameters and good electronic properties.[46] Through various efforts such as contact and structure optimizations,[139-141] SWNT-based field effect transistors (FETs) have been demonstrated to rival the state-of-art silicon FETs,[142-144] in some metrics. One proposed application is SWNT-FET based nonvolatile memory,[145-149] in which memory/conduction states are modulated and retained by trapped charges controlled through a third (gate) electrode. In the pursuit of high-density memory, conventional device scaling is expected to come up to a limit in the near future.[12] Two-terminal memory based on resistive switching materials are seen as an equivalent scaling to overcome this problem.[12] With the diameter of a SWNT comparable to that of a single filament in resistive switching materials,[148] a SWNT-based two-terminal memory could combine the merits of both simpler structure and small dimension.

Here we report reproducible current hysteresis in semiconducting SWCNTs in a two-terminal configuration without the third gate electrode. Based on hysteresis, bistable conduction states between low conductance and high conductance are achieved by applying voltage pulses of opposite polarities across the SWCNT, rendering a two-terminal nonvolatile memory device. Charge trapping at the SWCNT/SiO_x interface is proposed to account for the observed phenomena. This proposed mechanism is supported by the direct link between the switching behaviors and dominant charge carrier types (electrons or holes) in the SWCNTs. In particular, a transition in dominant carrier type induced by adsorption in air leads to the direct transition of hysteresis evolution in the same device, providing further evidence for the proposed mechanism.

6.2 Results and Discussion

6.2-1 Hysteresis and Memory Effect

A highly doped Si substrate ($\rho = 0.005\ \Omega\cdot cm$) with a 200 nm thick thermal SiO_2 layer (purchased from Silicon Quest International, Inc.) was used for SWCNT growth. At 975 °C, an ultralow-gas-flow chemical vapor deposition strategy (details can be found in Ref [150]) was adopted to grow long and sparsely aligned SWCNTs to facilitate device fabrications. The heights of the SWCNTs were determined by an ambient atomic force microscope (AFM) to be ~2 nm. Standard electron beam lithography was used, followed by metal depositions (40 nm thick Pt with a 5 nm

thick Ti adhesion layer) and a lift-off process to define the electrodes on top of the SWCNTs. Electrical characterizations were performed using an Agilent 4155C semiconductor parameter analyzer at room temperature under a vacuum of ~10^{-5} Torr (Desert Cryogenics model CPX, Lakeshore Cryotronics, Inc.), unless otherwise specified.

Fig. 81a shows a scanning electron microscope (SEM) image of a typical SWCNT device with an electrode–electrode spacing of ~1 μm. During a standard three-terminal measurement using the Si substrate as a back gate, the gate voltage (V_g) and drain current (I_{ds}) relationship exhibits typical p-type behavior (see Fig. 81b). The current level in the accumulation region (I_{on}) is close to the reported value using Pd contacts,[144] and the near-linear transport behavior (see inset in Fig. 81b) indicates good electrical contacts between the electrodes and the SWCNT.

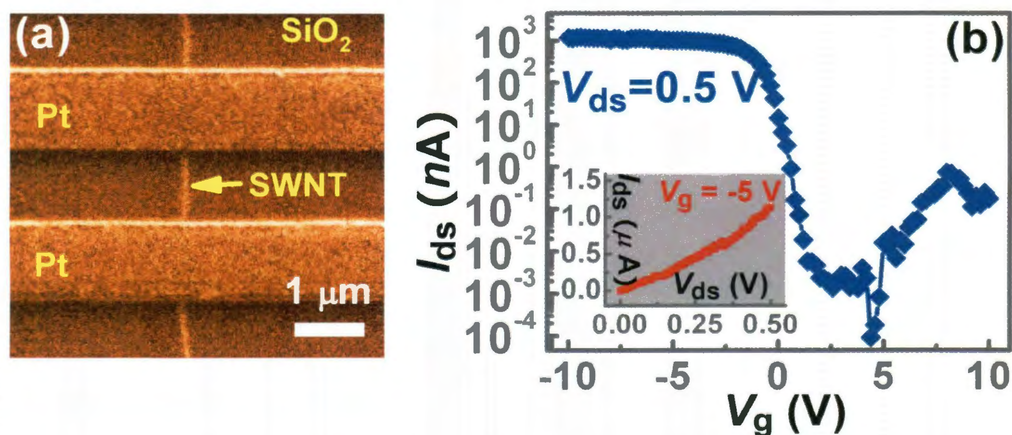


Figure 81 (a) An SEM image of a typical SWNT device. (b) I_{ds} – V_g curve of the SWNT device with V_g = 0.5 V. Inset: I_{ds} - V_{ds} curve with V_g = - 5 V.

For two-terminal measurements, the Si substrate with the SWCNT devices was put on a glass substrate with no back-gate electrode attached. Voltage sweeps were applied at one electrode with the other electrode grounded (see schematic in inset in Fig. 82a). Fig. 82a shows the typical current–voltage (I_{ds}–V_{ds}) evolution in the same SWCNT device as shown in Fig. 81. For convenience, I_{ds} is displayed in its absolute value $|I_{ds}|$, which also applies to the following figures. For a voltage sweep loop from 0 to +8 V and then back to 0 V (0 ⟶ +8 ⟶ 0 V, indicated by the arrows on the right side in Fig. 82a), the conduction of the SWCNT changes from a low-resistance (ON) state to a high-resistance (OFF) state, producing a current hysteresis. During the subsequent voltage sweep loop in the negative bias voltage region (0 ⟶ −8 ⟶ 0 V, indicated by the arrows on the left side in Fig. 82a), the conduction of SWCNT changes from an OFF state back to an ON state. This hysteretic behavior is reproducible during the subsequent series of voltage sweeps, and can be summarized as follows: a negative V_{ds} (*e.g.*, −8 V) across the SWCNT can "write" the device into an ON state, whereas a positive V_{ds} (*e.g.*, +8 V) can "erase" the device into an OFF state. Consequently, a two-terminal memory device can be realized by applying voltage pulses of −8 or +8 V across the SWCNT to write or erase the memory states. Fig. 82b demonstrates a series of memory cycles using voltage pulses of −8, +0.5, and +8 V, as writing, reading (5 times), and erasing operations, respectively. A bistable nondestructive read state with an ON–OFF ratio over 10^4 is achieved, which can also been inferred from the current hysteresis loops shown in Fig. 82a.

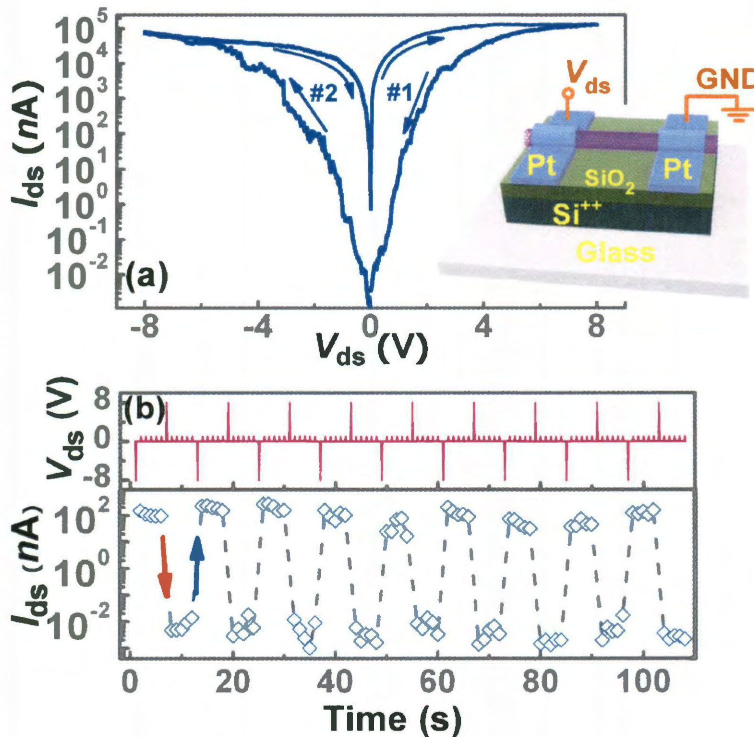


Figure 82 (a) Two-terminal current-voltage (I_{ds} - V_{ds}) evolution in the SWNT device. The arrows indicate the voltage sweep directions, and numbers indicate the sweep orders. Inset: Schematic of the two-terminal configuration for electrical measurements. (b) Top panel: a series of programming voltage pulses of -8 V and +8 V applied across the device. Between each two neighboring programming voltages, there are five voltage pulses of + 0.5 V as reading operations. All the pulse widths used are 300 ms. Bottom panel: corresponding memory states (I_{ds}) read out by the +0.5 V pulses shown in the top panel. The red arrow shows an erasing operation (from ON to OFF) by a +8 V pulse whereas the blue arrow shows a writing operation (from OFF to ON) by an -8 V pulse.

6.2-2 Mechanism Discussion

The good electrical contacts between the SWCNT and electrodes (see inset in

Fig. 81b) indicate that the conductance change does not result from electrical annealing of the contacts,[151] which would be irreversible. Other contact effects such as residual TiO_X switching[152] at the Pt/Ti/SWCNT interface can also be ruled out by the fact that devices with pure Pt electrodes still produce similar hysteresis and switching phenomena. The same amplitudes of voltage pulses used for both writing and erasing operations and the similar local heating due to current in the SWCNT during the two processes indicate that the effect is not due to heat-induced defeat healing[153,154] in the SWCNT. In fact, this kind of self-healing is irreversible in carbon nanotubes (CNTs)[154] or requires very sharp and short pulses (*e.g.*, < 100 ns) for the preparation of an OFF state in the amorphous carbon form.[155] This is in contrast to the reproducibility demonstrated in the present SWCNT device and longer pulses used at the millisecond level. It should be noted that here the SWCNT does not under go electrical breakdown, as opposed to the CNT-SiO_x-CNT nanogap switching system discussed in Chapter **2**.[52] In addition, here the switching in the SWCNT device works in a bipolar way (see Fig. 82b) where as that in SiO_x works in a unipolar way.

We propose that charge (electron) migration at the SWCNT/SiO_x interface is responsible for the observed hysteretic and switching behaviors. When a V_{ds} is applied across the device, an electric field component perpendicular to the SWCNT surface ($E_{\perp}$) is expected. A negative V_{ds} produces an $E_{\perp}$ pointing into the SWCNT (see illustration in Fig. 83a), dragging free electrons from the SWCNT to the SWCNT/SiO_x interface. The electrons are then trapped there and serve as an effective

negative gating, turning the p-type SWCNT into an ON state. Similarly, a positive V_{ds} produces an $E_{\perp}$ pointing out of the SWCNT (see illustration in Fig. 83b), which pulls the electrons from the SWCNT/SiO_x interface. The electron depleted SWCNT/SiO_x interface then works as an effective positive gating, turning the p-type SWCNT to an OFF state. This charge-trapping model is supported by the polarities of writing/erasing operations shown in Fig. 83b (indicated by blue and red arrows, respectively), in which a negative/positive V_{ds} pulse indeed produces the corresponding ON/OFF state as proposed.

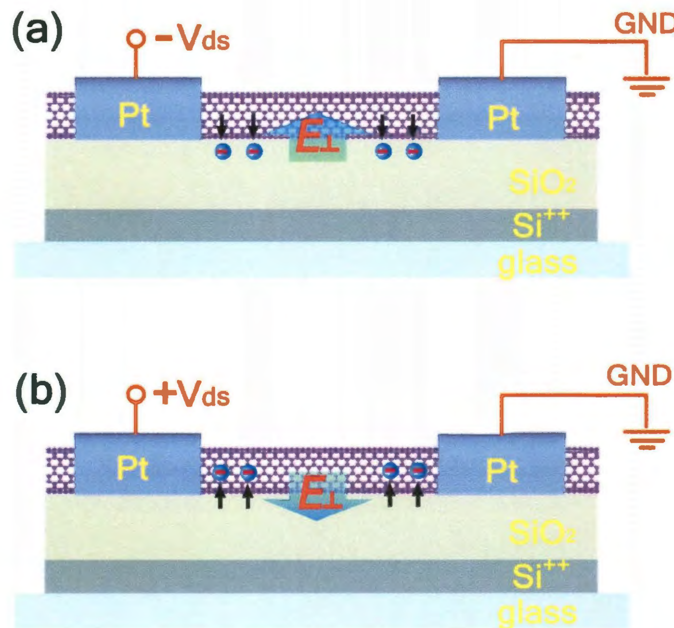


Figure 83. Schematic of charge (electron) transfer at the SWNT/ SiO_2 interface when a (a) negative or (b) positive V_{ds} is applied across the SWNT. The big blue arrows in the middle indicate the pointing directions of $E_{\perp}$ and the small black arrows indicate the direction of electron transfer.

The proposed mechanism is supported by the switching behaviors in an n-type SWCNT device (Fig. 84). Because of the opposite gating effect between n-type and p-type SWCNTs, it is straightforward to expect that a set of negative/positive voltages which writes/erases the p-type SWCNT into corresponding ON/OFF states will now do the opposite to erase/write the n-type SWCNT into OFF/ON states, respectively. Fig. 84a shows the evolution of current hysteresis in an n-type SWCNT. For a positive voltage sweep loop ($0 \rightarrow +12 \rightarrow 0$ V, see right side in Fig. 84a), the conduction of the SWCNT changes from an OFF state into an ON state, as opposed to that from ON to OFF in the p-type SWCNT (compare to right side in Fig. 82a). Similarly, the subsequent negative voltage sweep loop ($0 \rightarrow -12 \rightarrow 0$ V, see left side in Fig. 84a) features the opposite trend, too. The conduction of the SWCNT changes from an ON state to OFF state, as opposed to that from OFF to ON in the p-type SWCNT (see left side in Fig. 82a). Accordingly, this opposite hysteresis evolution compared to that in the p-type SWCNT is also reflected in the memory cycles (see middle panel in Fig. 84d), in which a positive programming V_{ds} pulse now becomes a writing operation, whereas a negative programming V_{ds} pulse becomes an erasing one.

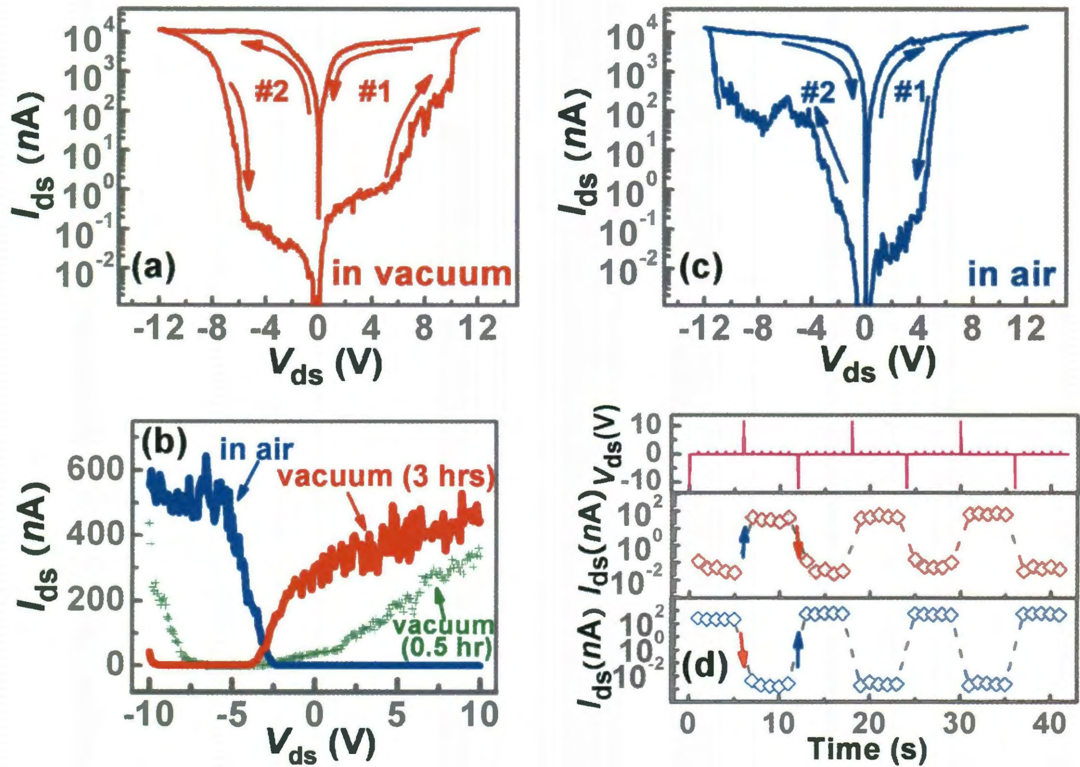


Figure 84 (a) Two-terminal I_{ds} - V_{ds} evolution in a second SWNT device in vacuum (pumping down for 3 h). The arrows indicate the voltage sweep directions and the numbers indicate the sweep orders. (b) $I_{ds} - V_g$ (SWNT-type) transition in the same device. The red curve was measured in vacuum environment (pumping down for 3 hrs), showing dominant n-type behavior (corresponding to (a)). The blue curve was measured in ambient environment after 24-hr exposure to air, showing p-type behavior (corresponding to (c)). The green curve shows intermediate ambipolar behavior in vacuum (pumping down for 0.5 h). (c) I_{ds} - V_{ds} evolution of the device in ambient environment after 24 h exposure to air. (d) Top panel: a series of programming voltage pulses of -12 V and +12 V. Between each two neighboring programming voltages, there are five voltage pulses of + 0.5 V as reading operations. The corresponding memory states (I_{ds}) read out by the +0.5 V pulses are shown in middle panel (in vacuum, pumping down for 3 hrs) and bottom panel (in air). The blue and red arrows show writing and erasing operations, respectively.

The transition of the switching behaviors in the same device, as a result of SWCNT n- to p-type change, discounts individual device variations from consideration and provides added evidence for the proposed mechanism. The electrical measurements of the device shown in Fig. 84a were done in vacuum (~10^{-5} Torr) after pumping for 3 h. Besides the dominant n-type transport behavior, there is also a visible p-type tail in the negative gate voltage region (see red curve in Fig. 84b), showing ambipolar[156] trait. Exposing the device in air for 24 h leads to the suppression of the n-type transport and the enhancement of p-type transport (see blue curve in Fig. 84b), resulting in a SWCNT-type transition into p-type behavior due to oxygen adsorption.[157] During the subsequent measurements in ambient environment using the two-terminal configuration as described before, the evolution of the current hysteresis (see Fig. 84c) acquires a reverse trend compared to that observed in vacuum (see Fig. 84a), becoming that of a typical p-type device as described previously in Fig. 82a. This SWCNT-type transition induced reversal in hysteresis evolution is again reflected in the corresponding memory cycles, in which a negative/positive V_{ds} pulse that previously erases/writes the device into OFF/ON state in vacuum (see middle panel in Fig. 84d) now writes/erases the device into ON/OFF in air (see bottom panel in Fig. 84d).

Not surprisingly, current hysteresis was not observed in metallic SWCNTs because of their intrinsic insensitivity to gating (see Fig. 85). This distinguishes the

conductance change in our SWCNT devices from phase transition behaviors observed in metallic SWCNTs by electron irradiation[158,159] or by molecular assembly.[160] No phase transition, for example, between semiconducting and metallic states, was observed in our SWCNT devices. The switching SWCNTs retain their semiconducting properties during different memory states, which was confirmed by standard three-terminal measurements using the Si substrate as a back gate.

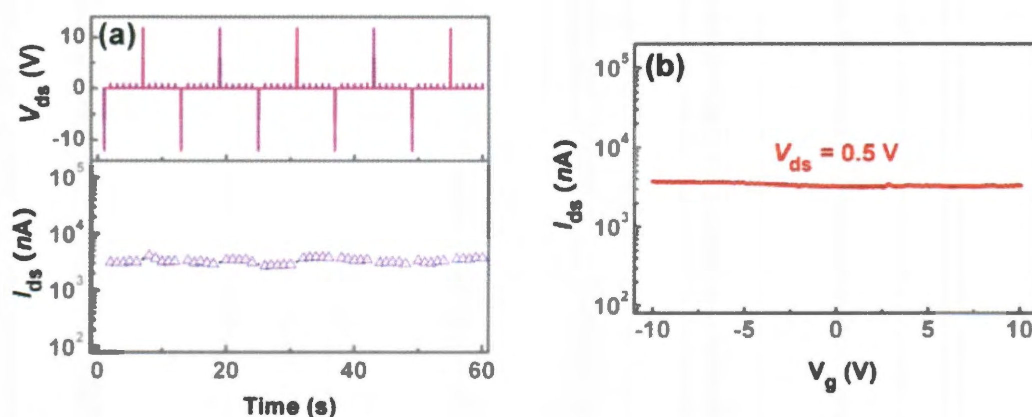


Figure 85. (a) Top panel: a series of programming voltage pulses of -12 V and +12 V applied across a metallic SWCNT device. Between each two neighboring programming voltages, there are five voltage pulses of + 0.5 V as reading operations. Bottom panel: corresponding memory states (I_{ds}) read out by the +0.5 V pulses shown in the top panel. (b) $I_{ds} - V_g$ curve of the metallic SWCNT.

The reproducibility of the current hysteresis was further tested by memory cycling in vacuum. The SWCNT device shows no obvious degradation after 1000 continuous cycles (see Fig. 86a), indicating good memory durability during programming. The stored conduction states show a nonvolatile property with the

retention time dependent on the environment. The conductance of an OFF state increases ~3 orders of magnitude after ~5 h in an ambient environment (see red curve in Fig. 86b), whereas it only increases ~1 order of magnitude after 15 h in vacuum (see green dashed curve in Fig. 86b). This is consistent with the charge-trapping mechanism since atmospheric water has been reported to assist in the discharging process at the SWCNT/SiO_2 interface.[161,162] Meanwhile, the conductance of an ON state only shows a small decrease after a 7 h air exposure (see blue curve in Fig. 86b), and retains a similar value afterward (*e.g.*, after 30 d in air). The retention time in the ON state, exceeding the charge storage stability of the reported 14 days,[141,145] indicates that the pristine conduction state of the SWCNT is close to an ON state, which may be due to a constant gate threshold voltage shift commonly observed in SWCNTs. This supplements the proposed mechanism such that, instead of having to charge/discharge the SWCNT/SiO_2 interface along the entire SWCNT, local charge trapping can now pinch off the device, while discharging this local region can bring the device back to the ON state.

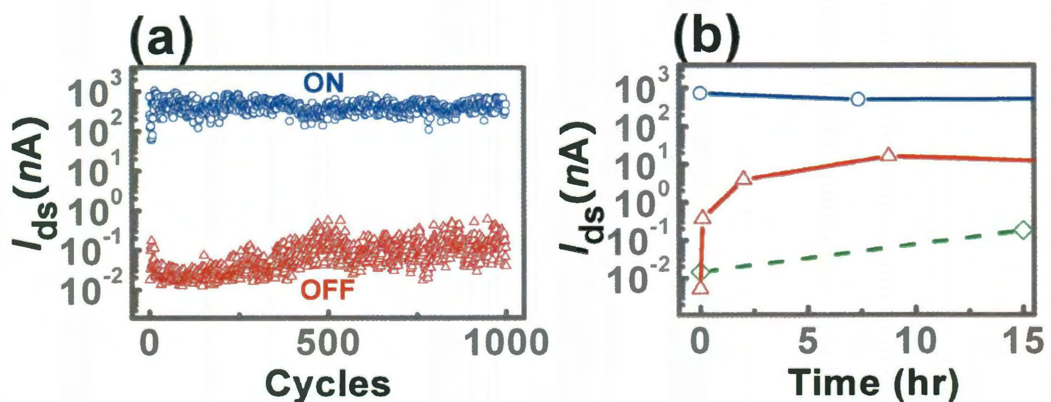


Figure 86. (a) 10^3 memory cycles in a SWNT device using -12 V, +12 V, and +0.5 V

as writing, erasing, and reading operations, respectively. (b) Retention of memory states in ambient environment for ON (blue curve) and OFF (red curve) states. The dashed green curve shows the decay of the OFF state in vacuum.

6.2-3 Charge-Based Current Hysteresis in Other Materials

Based on the mechanism discussed above, this kind of current hysteresis should be observed in many different semiconducting materials on the conditions that: (a) the material forms a good interface with the dielectric substrate so that a sufficient charge-trap medium is provided and (b) the semiconductor is thin so that the interface charge can affect the overall transport. In this regard, semiconducting nanomaterials such as nanowires and 2-dimensional materials are good candidates for this effect. Some charge-trapping medium could be introduced in between the semiconductor and substrate to enhance the effect.[163]

Here we show another example in a graphene device. Mon or bilayered graphene was produced by mechanical exfoliation[164] on a highly doped silicon substrate capped with 300 nm thermal SiO_x layer. The thickness of the graphene layer was confirmed by combined SEM and AFM measurements. Note that during mechanical exfoliation, graphene nanoribbons (GNRs) at the width of 20 – 100 nm could be readily produced (Fig. 87a). The defects and adsorption usually affect the symmetric bipolar transport property in graphene,[165] therefore negative and positive charge trapping can still produce different conductance modulation. Fig. 87b,c shows the current hysteresis

and memory effect in the graphene device in a two-terminal configuration without the third gate electrode. The ON/OFF ratio is comparatively low because of the *zero* bandgap structure in graphene. This narrow bandgap could be increased by laterally confinement in the graphene stripe,[166] hence increasing the ON/OFF ratio.

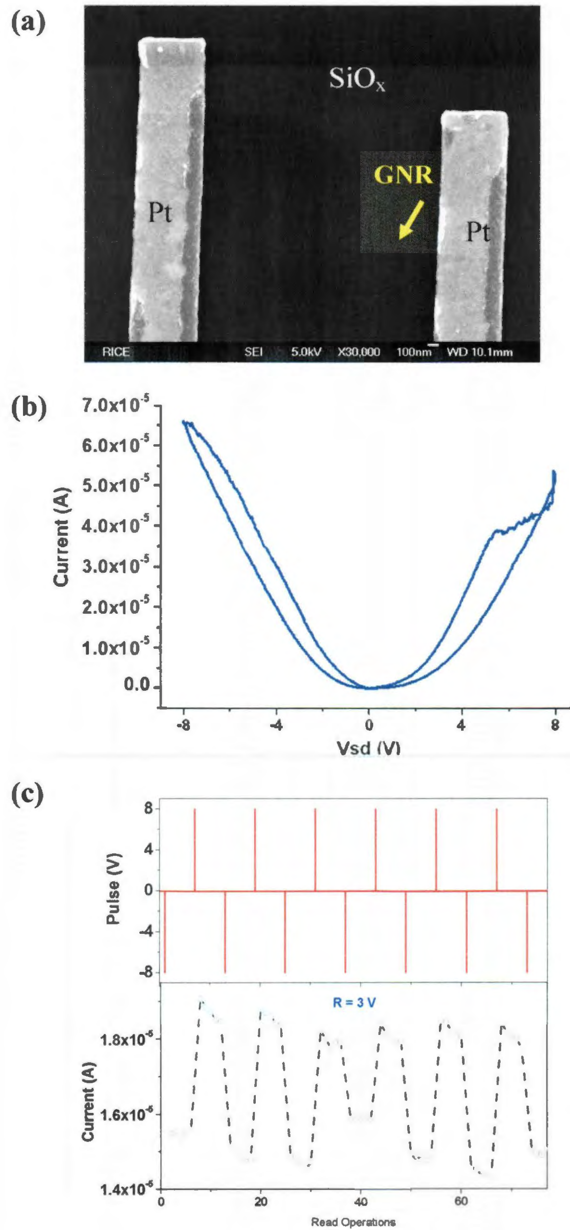


Figure 87. Current hysteresis and two-terminal memory effect in graphene. (a) SEM

image of an exfoliated GNR connected by two Pt electrodes. (b) Current hysteresis in the device. (c) Memory cycles in the graphene device using -8 V, +8 V, and + 1 V as writing, erasing, and reading operations, respectively. The programming current is not shown here.

For this reason, caution should be paid when studying resistive switching materials in a planar structure on an insulating substrate. Many resistive switching materials are pristinely semiconducting.[12] The charge effect at the material/dielectric interface could produce hysteresis and memory effects in the two-terminal configuration as discussed above. The two phenomena could be mixed[167] when the resistive switching effect in the material works in a bipolar manner as does the charge effect. However, mechanistically the two are very different processes.

6.3 Summary

In summary, current hysteresis is observed in semiconducting SWCNTs. A two-terminal nonvolatile memory is demonstrated on the basis of the hysteresis. The direct link between the hysteretic/switching behaviors and SWCNT types supports a mechanism in which charge trapping at the SWCNT/SiO_x interface is the most likely cause. A similar effect is demonstrated in a GNR device.

7. List of References

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8. Appendix

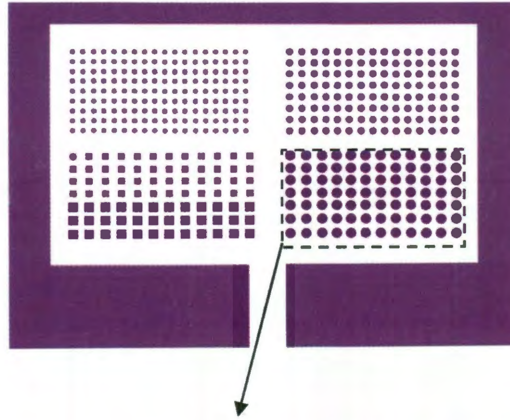
I. polySi-SiO_x-polySi (40 nm) devices for NASA HiMassSEE test

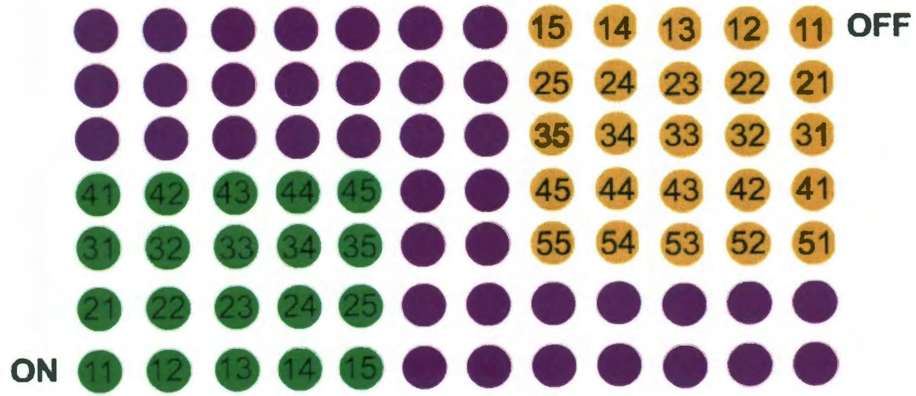
200 devices on 4 separate chips, with 110 set to ON and 90 set to OFF, were prepared. The yield is **99.5%** (200/201 – only 1 out of 200 was not electroformed because it was initially in a full-conduction state). Each device was cycled several tens of times before collecting the memory-state data. Below are the details of device layout and corresponding memory states.

Chip #1:

Specification: Dry etching with Cr layer as sacrificial mask (Cr removed by CEP-200). The chip was annealed in vacuum (~ 7 mTorr) at 450 °C for 5 min. Electrical testing vacuum level at ~ 6×10^{-3} mTorr.

Device layout for chip #1 (device size 100 μm in diameter):





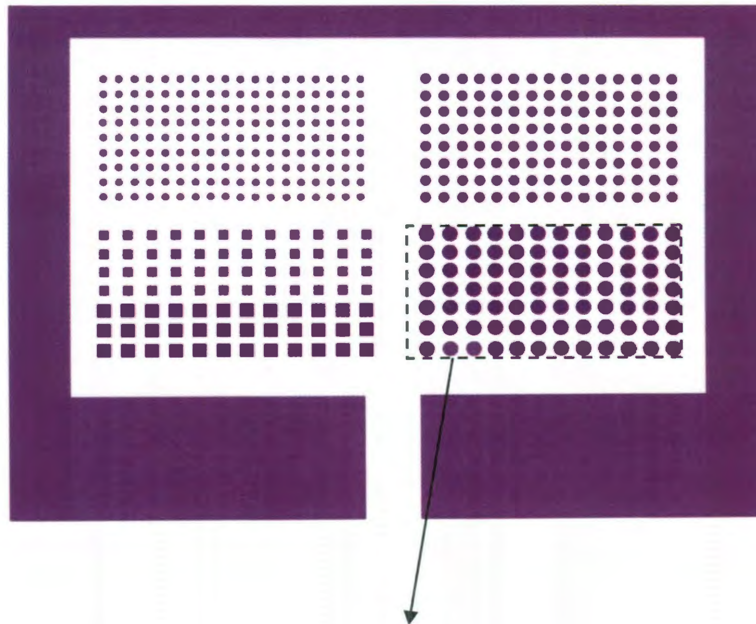
Corresponding memory states for chip #1 (read at + 1 V pulse):

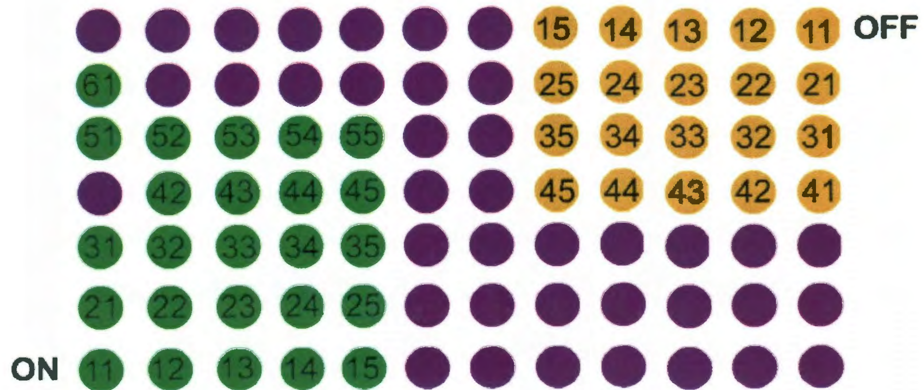
ON Devices			OFF Devices	
Dev#	I@ + 1 V (A)		Dev#	I@ + 1 V (A)
11	9.876800E-7		11	5.173300E-9
12	2.089900E-6		12	5.769000E-11
13	2.092800E-6		13	2.980500E-10
14	4.535000E-6		14	5.183600E-10
15	3.582800E-6		15	3.100700E-10
21	3.349800E-6		21	4.209500E-9
22	3.185000E-6		22	2.903000E-11
23	1.393500E-6		23	1.218000E-11
24	9.821400E-7		24	7.780000E-12
25	4.451700E-7		25	3.402000E-11
31	1.826500E-6		31	3.459800E-10
32	4.026600E-6		32	1.165700E-10
33	3.921700E-6		33	1.118000E-11
34	1.427800E-6		34	1.642000E-11
35	2.482900E-6		35	1.504000E-11
41	1.869600E-6		41	8.907000E-11
42	1.044500E-6		42	1.930000E-11
43	1.499800E-6		43	1.176000E-11
44	1.071000E-6		44	1.600800E-10
45	1.924900E-6		45	7.911000E-11
			51	1.060000E-11
			52	8.325000E-11
			53	1.810000E-11
			54	3.810800E-10
			55	4.060000E-12

Chip #2:

Specification: Dry-etching with Cr layer as sacrificial mask (Cr removed by CEP-200). The chip was annealed in vacuum (~ 6 mTorr) at 400 °C for 6 min. Electrical testing vacuum level at ~ 6×10^{-3} mTorr.

Device layout for chip #2(device size 100 µm in diameter):





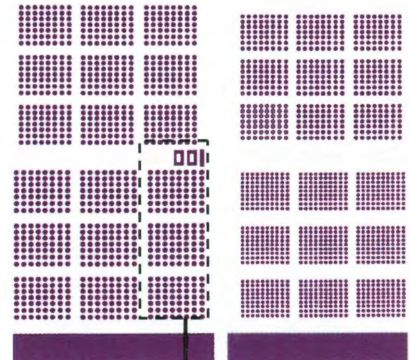
Corresponding memory states for chip #2 (read at + 1 V pulse):

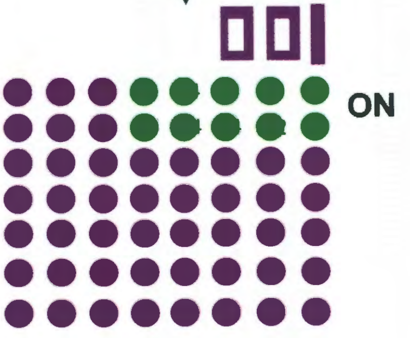
ON Devices			OFF Devices	
Dev #	*I* @ + 1 V (A)		Dev #	*I* @ + 1 V (A)
11	1.564000E-5		11	1.673100E-10
12	1.571400E-6		12	3.781400E-10
13	1.184000E-5		13	8.407000E-11
14	5.913900E-6		14	2.788000E-11
15	2.105900E-7		15	1.922000E-11
21	1.358200E-6		21	3.540000E-11
22	8.584700E-7		22	4.740000E-11
23	1.470000E-6		23	7.760000E-12
24	1.145300E-6		24	8.130000E-12
25	2.717500E-7		25	3.990500E-10
31	1.255400E-6		31	1.285000E-11
32	7.713000E-6		32	1.009100E-10
33	6.885300E-7		33	4.107000E-11
34	2.663100E-6		34	2.261000E-10
35	1.829600E-6		35	6.600000E-13
42	5.987300E-6		41	2.600000E-12
43	1.304200E-6		42	2.190000E-12
44	5.281100E-6		43	3.195500E-10
45	2.838000E-6		44	1.366200E-9
51	5.731300E-6		45	3.090000E-11
52	1.972400E-6			
53	1.543400E-6			
54	1.454100E-6			
55	1.237300E-6			
61	8.618900E-7			

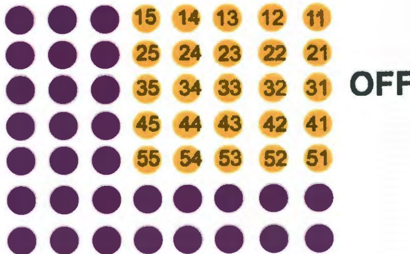
Chip #3:

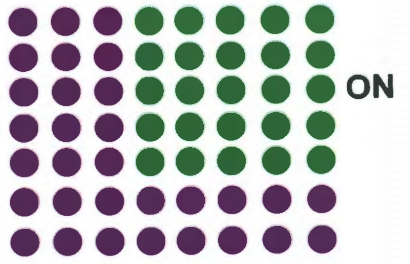
Specification: Dry-etching with Cr layer as sacrificial mask (Cr removed by CEP-200). The chip was annealed in vacuum (~ 6 mTorr) at 450 °C for 5 min. Electrical testing vacuum level at ~ 6×10^{-3} mTorr.

Device layout for chip #3 (device size 100 μm in diameter):









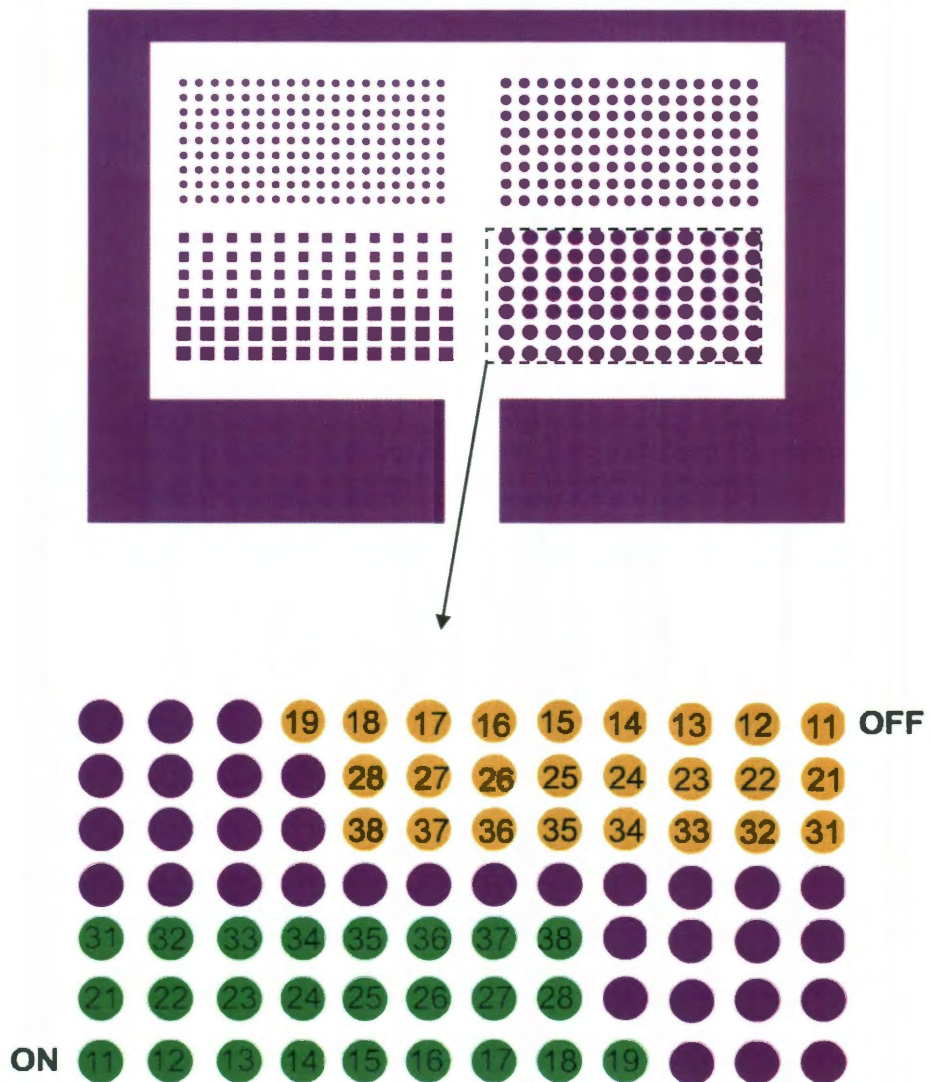
Corresponding memory states for chip #3 (read at + 1 V pulse):

ON Devices					OFF Devices	
Dev #	I @ + 1 V (A)	Dev #	I @ + 1 V (A)		Dev #	I @ + 1 V (A)
A1	4.267600E-7	11	1.356600E-6		11	1.841000E-11
A2	7.511000E-7	12	1.248400E-6		12	1.848900E-10
A3	5.898600E-7	13	2.361400E-6		13	1.381000E-11
A4	2.662700E-6	14	1.075400E-6		14	2.631200E-10
A5	2.124600E-6	15	1.099300E-6		15	3.610800E-10
B1	1.269300E-6	21	1.316600E-6		21	1.307300E-10
B2	1.513000E-6	22	6.704700E-7		22	3.163000E-11
B3	5.332500E-7	23	4.074200E-7		23	1.358000E-11
B4	1.453100E-6	24	2.072900E-6		24	5.264000E-11
B5	1.218400E-6	25	1.199500E-6		25	1.225000E-11
		31	1.827100E-6		31	1.401000E-11
		32	1.772000E-6		32	2.214000E-11
		33	3.468200E-6		33	7.340000E-11
		34	1.296700E-6		34	2.843700E-10
		35	2.032000E-6		35	5.490000E-12
		41	1.265900E-6		41	2.160000E-10
		42	2.890300E-6		42	6.833000E-11
		43	1.144100E-6		43	7.070000E-12
		44	2.642400E-6		44	1.190000E-11
		45	5.533800E-6		45	6.440000E-12
		51	2.712600E-6		51	8.514000E-11
		52	1.188400E-6		52	3.590000E-12
		53	7.411300E-6		53	1.236000E-11
		54	2.222700E-6		54	1.370000E-9
		55	1.977600E-6		55	2.731000E-11

Chip #4:

Specification: Dry etching with photoresist (S-1813) as sacrificial mask (photoresist removed by 10 s acetone rinse along with ultra-sonication). No annealing performed. Electrical testing was at vacuum level at ~ 6×10^{-3} mTorr.

Device layout for chip #4 (device size 100 μm in diameter):



Corresponding memory states for chip #4 (read at + 1 V pulse):

ON Devices			OFF Devices	
Dev #	*I* @ + 1 V (A)		Dev #	*I* @ + 1 V (A)
11	1.452500E-6		11	3.198000E-11
12	1.114300E-6		12	8.613000E-11
13	1.152300E-6		13	8.000000E-13
14	1.139300E-6		14	7.430000E-11
15	1.284400E-6		15	5.710000E-12
16	1.674600E-6		16	2.587000E-11
17	2.253500E-6		17	5.000000E-13
18	6.849400E-7		18	1.735000E-11
19	1.104000E-6		19	4.392000E-11
21	1.443400E-6		21	1.372000E-11
22	1.913300E-6		22	1.226000E-11
23	2.675700E-6		23	1.851000E-11
24	2.298800E-6		24	2.720000E-12
25	2.736500E-6		25	5.584800E-10
26	7.261600E-7		26	2.345100E-10
27	3.845000E-7		27	1.265000E-11
28	1.136500E-6		28	3.540000E-12
31	1.578200E-6		31	2.751000E-11
32	8.014300E-7		32	1.497000E-11
33	5.124800E-7		33	1.215000E-11
34	1.650200E-6		34	5.113000E-11
35	4.259400E-7		35	5.250400E-10
36	7.831800E-7		36	1.081000E-11
37	1.303100E-6		37	6.430000E-12
38	1.293000E-6		38	1.611600E-10

II. Design of the TEM Holder for *in situ* Electrical Measurement

The TEM holder (for JEM 2100F system) includes three parts (schematic I) s: (1) the TEM stage, (2) the hollow long rod and (3) handle. The electrical wiring is through the hollow rod to the stage with sealing at the handle end.

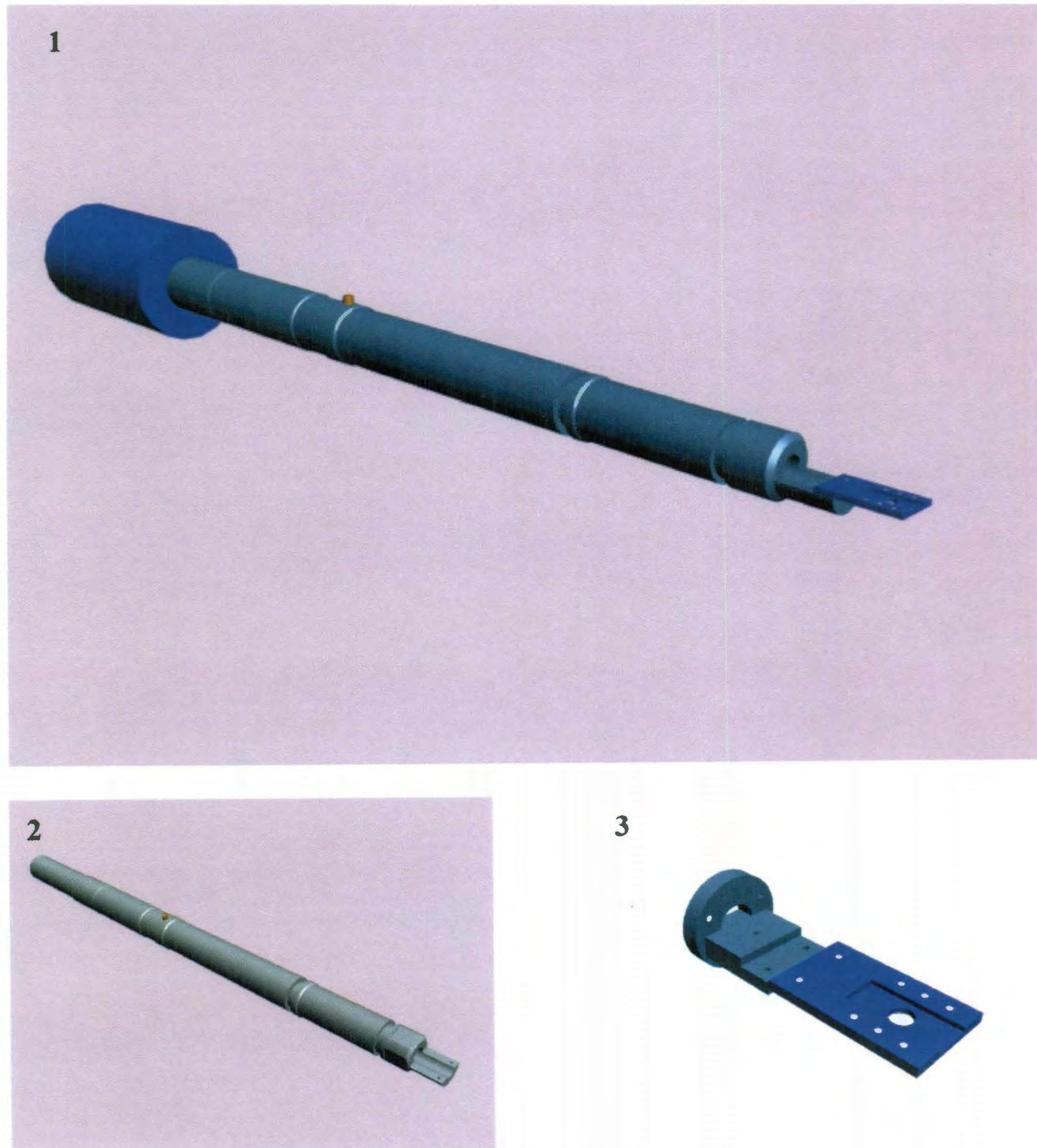


Figure I. Illustration of the home-made TEM holder. (1) The overall assembly, (2) the rod structure and (3) the imaging stage.

The detailed parameters of the long rod (Fig. I-2) and stage (Fig. I-3) are as follows.